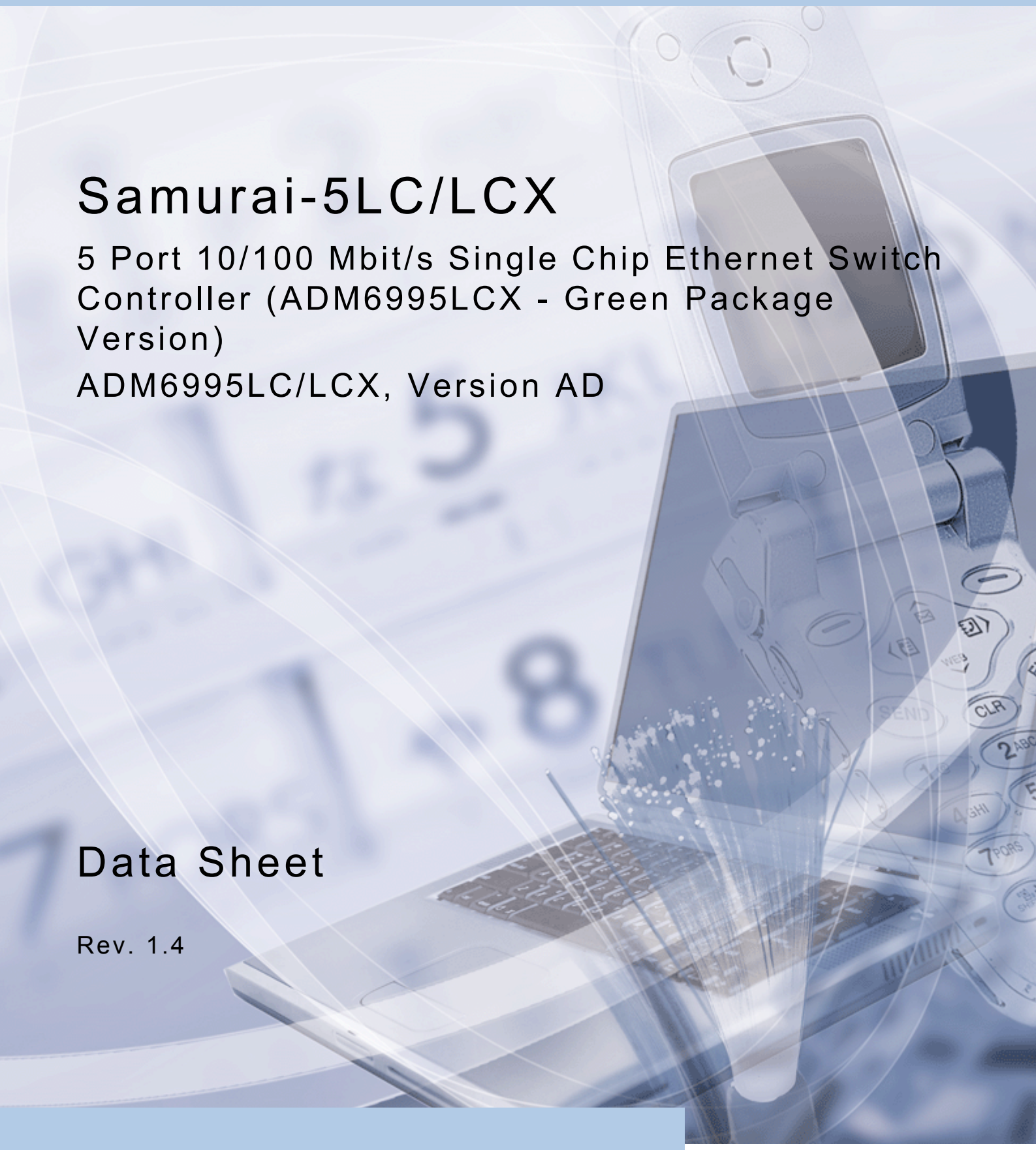
March 2006

Samurai-5LC/LCX

5 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6995LCX - Green Package Version)

ADM6995LC/LCX, Version AD



Data Sheet

Rev. 1.4

Communication Solutions

Never stop thinking

Edition 2006-03-16

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ADM6995LC/LCX 5 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6995LCX - Green Package Version)

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	Rev. 1.15, Changed to Infineon format
Page 33	Rev. 1.2, Modify EEPROM register 31_H map and have more clear port base priority description
2005-08-30	Rev. 1.3, Update in content
2005-11-03	Revision 1.3 changed to Revision 1.31 Minor change. Included Green package information
2006-03-16	Revision 1.31 changed to Revision 1.4 Add thermal resistance information

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1 Product Overview

1.1 Overview

The Samurai-5LC/5LCX (ADM6995LC/LCX) is a high performance, low cost, highly integrated (Controller, PHY and Memory) five-port 10/100 Mb/s TX/FX with all ports supporting 10/100 Mbit/s Full/Half duplex. The Samurai-5LC/5LCX (ADM6995LC/LCX) is intended for applications such as stand alone bridges for the low cost SOHO market such as 5 Port Switch. The Samurai-5LCX (ADM6995LCX) is the environmentally friendly “green” package version.

Samurai-5LC/5LCX (ADM6995LC/LCX) provides many advanced functions such as: **802.1p(Q.O.S.), Port-based/Tag-based VLAN, Port MAC address Locking, Management, Port Status & TP Auto-MDIX**.

The Samurai-5LC/5LCX (ADM6995LC/LCX) also supports Back Pressure in Half-Duplex mode and 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffer is full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the Samurai-5LC/5LCX (ADM6995LC/LCX) will issue a JAM pattern on the receiving port in Half Duplex mode and issue the 802.3x Pause packet back to the receiving end in Full Duplex mode.

The built-in SRAM used for packet buffering is divided into 256 bytes/block to achieve the optimized memory utilization through complicated link lists on packets with various lengths.

Samurai-5LC/5LCX (ADM6995LC/LCX) also supports priority features by Port-Base, VLAN and IP TOS field checking. Users can be easily set different priority modes in individual ports, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports four queues in the way of fixed 8:4:2:1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and Data. Tag/Untag, and up to 16 groups of VLAN also is supported.

An intelligent address recognition algorithm allows Samurai-5LC/5LCX (ADM6995LC/LCX) to recognize up to 2K different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by Samurai-5LC/5LCX (ADM6995LC/LCX) to use on Building Internet access to prevent multiple users sharing one port traffic.

1.2 Features

- Supports five 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces.
- Supports 2K MAC addresses table with 4-ways associative hash algorithm.
- 6KX64 bits packet buffers are divided into 192 blocks of 256 bytes each
- Supports four queue for QoS
- Supports priority features by Port-Based, 802.1p, IP TOS of packets.
- Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.
- Supports buffer allocation with 256 bytes per block
- Supports Aging function Enable/Disable.
- Supports per port Single/Dual color mode with Power On auto diagnostic.
- Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- Supports Back Pressure function for Half Duplex operation in case buffer is full.
- Supports packet length up to 1518/1522 (Default)/1536/1784 bytes in maximum.
- Broadcast/Multicast Storm Suppression.
- Supports Tag-based VLAN. Up to 16 VLAN groups is implemented by the last four bits of VLAN ID.
- 2bit MAC clone to support multiple WAN application
- Supports TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Easy Management 32bits smart counter for per port RX/TX byte/packet count, 16-bit smart counter for per port ERROR count and Collision count.

- Support PHY status output for management system.
- 25M Crystal only for the whole system.
- 128 QFP package with 0.18 μm technology. 1.8 V/3.3 V power supply.
- 1.0 W low power consumption.

1.3 Applications

Samurai-5LC/5LCX (ADM6995LC/LCX) in 128-pin PQFP:

- SOHO 5-port switch

1.4 Block Diagram

Figure 1 below shows a simple block diagram of the Samurai-5LC/5LCX (ADM6995LC/LCX) internal blocks.

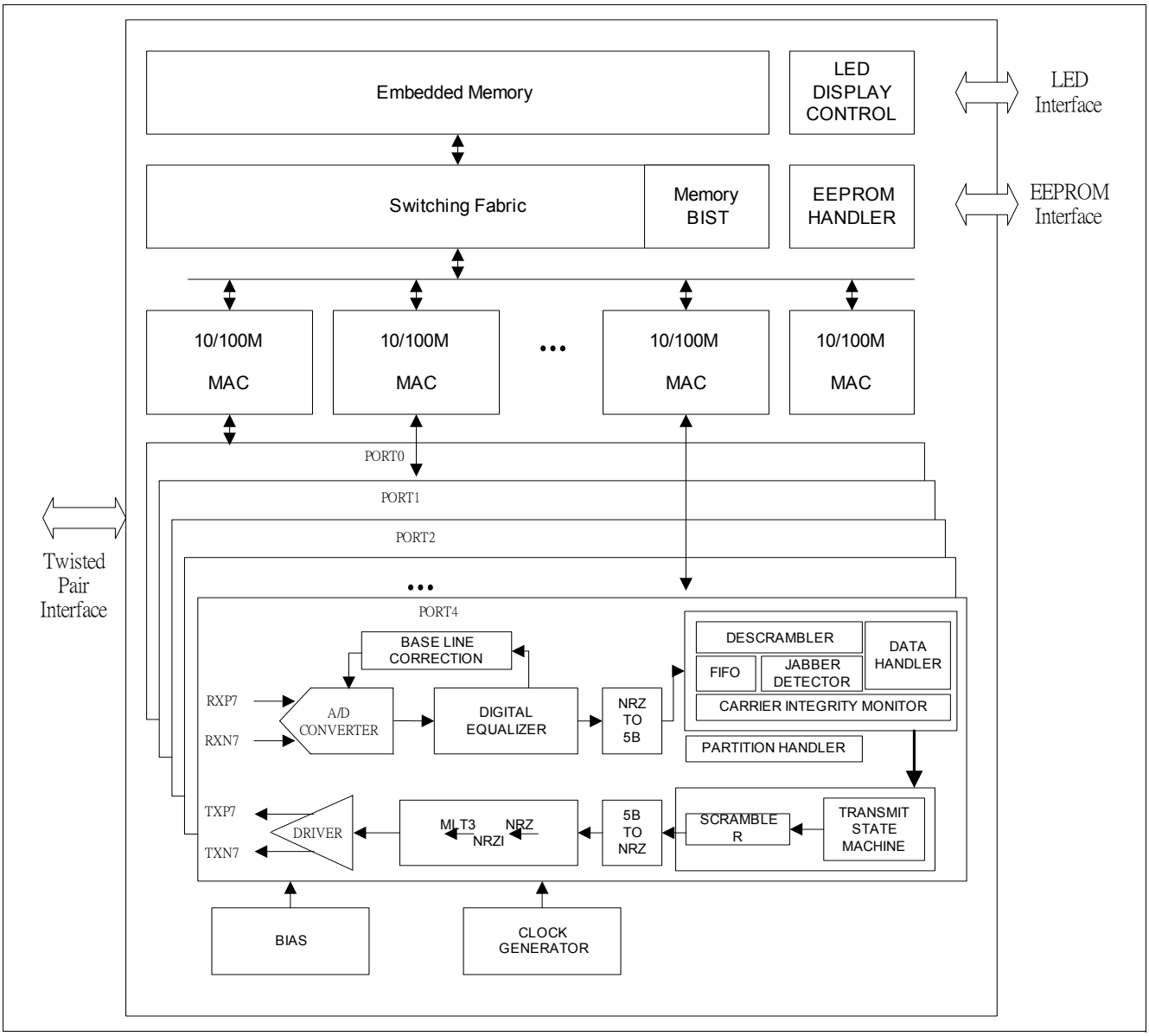


Figure 1 Samurai-5LC/5LCX (ADM6995LC/LCX) Block Diagram

2 Interface Description

This chapter describes the interface descriptions for the Samurai-5LC/5LCX (ADM6995LC/LCX)

- Pin Diagram
- Abbreviations
- Pin Description by Function

2.1 Pin Diagram

Figure 2 shows the pin diagram for the Samurai-5LC/5LCX (ADM6995LC/LCX).

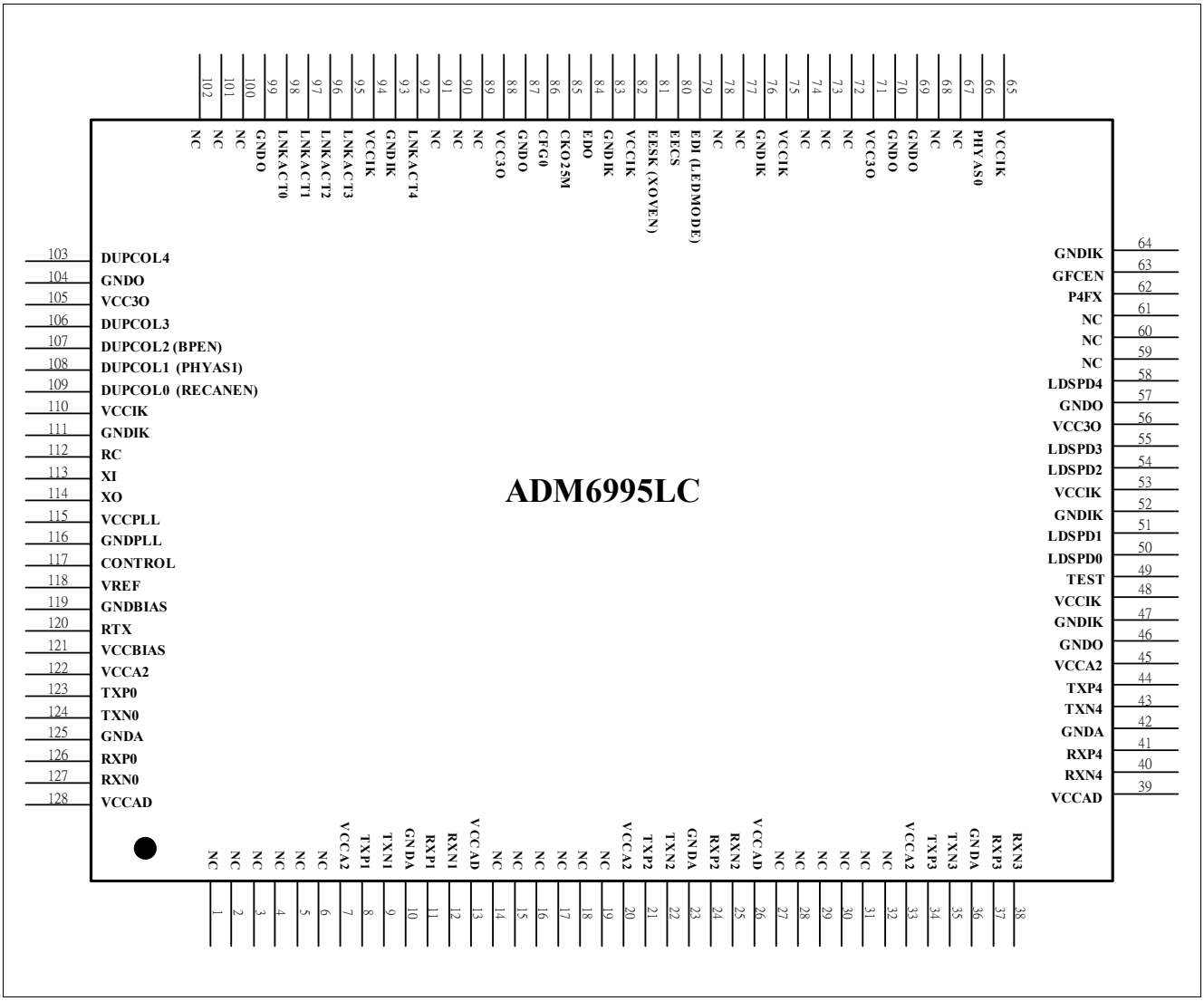


Figure 2 5 TP/FX PORT 128 Pin Diagram

2.2 Abbreviations

Standard abbreviations for I/O tables:

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU	Pull up, 10 kΩ
PD	Pull down, 10 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Description by Function

Samurai-5LC/5LCX (ADM6995LC/LCX) pins are categorized into one of the following groups:

- Network Media Connection
- LED Interface
- EEPROM Interface
- Power/Ground, 48 pins
- Miscellaneous

*Note: **Table 1** can be used for reference.*

Table 3 IO Signals

Ball No.	Name	Pin Type	Buffer Type	Function
Network Media Connection				
41	RXP_4	AI/O	ANA	**Receive Pair** Differential data is received on this pin.
37	RXP_3			
24	RXP_2			
11	RXP_1			
126	RXP_0			
40	RXN_4	AI/O	ANA	
38	RXN_3			
25	RXN_2			
12	RXN_1			
127	RXN_0			
44	TXP_4	AI/O	ANA	**Transmit Pair** Differential data is transmitted on this pin.
34	TXP_3			
21	TXP_2			
8	TXP_1			
123	TXP_0			
43	TXN_4	AI/O	ANA	
35	TXN_3			
22	TXN_2			
9	TXN_1			
124	TXN_0			
LED Interface				
103	DUPCOL4	O	8 mA, PD, LVTTL	**Port 4 Duplex /Collision LED** In Full duplex mode, this pin acts as DUPLEX LED for port 4, respectively; in half duplex mode, it is collision LED for each port. See **Chapter 3.20 LED Display** for more detail.
106	DUPCOL3	O	8 mA, PD, LVTTL	**Port 3 Duplex /Collision LED** In Full duplex mode, this pin acts as DUPLEX LED for port 3, respectively; in half duplex mode, it is collision LED for each port. See **Chapter 3.20 LED Display** for more detail.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
107	BPEN	I	PU, LVTTL	**Recommend Back-Pressure in Half-Duplex** Value on this pin will be latched by Samurai-5LC/5LCX (ADM6995LC/LCX) during power on reset as the beck-pressure enable in half-duplex mode. *Note: Power On Setting* 0_B Disable Back-Pressure 1_B Enable Back-Pressure
	DUPCOL2	O	8 mA, PU, LVTTL	**Port 2 Duplex-collision LED** In Full duplex mode, this pin acts as port 2 DUPLEX LED; in half duplex mode, it is collision LED for port 2. See **Chapter 3.20 LED Display** for more detail.
108	PHYAS1	I	PD, LVTTL	**Recommend PHY Address Bit 1** Value on this pin will be latched by Samurai-5LC/5LCX (ADM6995LC/LCX) during power on reset as the PHY address recommend value bit 1. See **PHYAS0** description for more detail. *Note: Power On Setting*
	DUPCOL1	O	8 mA, PD, LVTTL	**Port 1 Duplex-collision LED** In Full duplex mode, this pin acts as port 1 DUPLEX LED; in half duplex mode, it is collision LED for port 1. See **Chapter 3.20 LED Display** for more detail.
109	RECANEN	I	PU, LVTTL	**Recommend Auto Negotiation Enable** Only valid for Twisted pair interface. Programmed this bit to 1 has no effect to Fiber port. *Note: Power On Setting.* 0_B Disable all TP port auto negotiation capability 1_B Enable all TP port auto negotiation capability
	DUPCOL0	O	8 mA, PU, LVTTL	**Port 0 Duplex-collision LED** In Full duplex mode, this pin acts as port 0 DUPLEX LED; in half duplex mode, it is collision LED for port 0. See **Chapter 3.20 LED Display** for more detail.
92	LNKACT_4	O	8 mA, PD, LVTTL	**LINK/Activity LED of Port 4 to 0** Used to indicate corresponding port' s link/activity status, see **Chapter 3.20 LED Display** for more detail.
95	LNKACT_3			
96	LNKACT_2			
97	LNKACT_1			
98	LNKACT_0			
58	LDSPD_4	O	8 mA, PD, LVTTL	**Port 4 to Port 0 Speed LED** Used to indicate corresponding port' s speed status, see **Chapter 3.20 LED Display** for more detail.
55	LDSPD_3			
54	LDSPD_2			
51	LDSPD_1			
50	LDSPD_0			
EEPROM Interface				

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
84	EDO	I	PU, LVTTL	**EEPROM Data Output** This pin is used to input EEPROM data when reading EEPROM. During Samurai-5LC/5LCX (ADM6995LC/LCX) initialization, Samurai-5LC/5LCX (ADM6995LC/LCX) will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See **Chapter 4.6 EEPROM Access** for more detail.
80	IFSEL	I	PD, LVTTL	**Interface Selection** After Samurai-5LC/5LCX (ADM6995LC/LCX) initialization process is done, this pin is used to select using EEPROM interface or SDC/SDIO interface. EECS/IFSEL interface 0_B SDC/SDIO interface 1_B EEPROM interface
	EECS	O	4 mA, PD, LVTTL	**EEPROM Chip Select** During Samurai-5LC/5LCX (ADM6995LC/LCX) initialization, this pin is used as EEPROM chip select signal. During Samurai-5LC/5LCX (ADM6995LC/LCX) initialization, Samurai-5LC/5LCX (ADM6995LC/LCX) will drive EEPROM interface signal to read settings from EEPROM. Any other devices attach to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See **Chapter 4.6 EEPROM Access** for more detail.
81	XOVEN	I	PD, LVTTL	**Cross Over Enable** Value on this pin (active low) will be latched by Samurai-5LC/5LCX (ADM6995LC/LCX) at the rising edge of RESETL for port 4~0 crossover auto detect (Only available in TP interface). *Note: Power On Setting.* 0_B Disable 1_B Enable
	EESK	I/O	4 mA, PD, LVTTL	**EEPROM Serial Clock** During Samurai-5LC/5LCX (ADM6995LC/LCX) initialization, this pin is used to output clock to EEPROM. After Samurai-5LC/5LCX (ADM6995LC/LCX) initialization process is done, this pin is used as EEPROM interface clock input if **IFSEL** = 1.
	SDC	I	PD, LVTTL	**Serial Management interface Clock input** If **IFSEL** = 0, this pin is used as serial management interface clock input.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
79	LED_MODE	I	PD, LVTTL	**Enable Mac to Choose LED Display Mode** Value on this pin will be latched by Samurai-5LC/5LCX (ADM6995LC/LCX) at the rising edge of RESETL as Dsingle/dual color LED mode control signal. See **Chapter 3.20 LED Display** for more detail. *Note: Power On Setting.*
	EDI	I/O	8 mA, PD, LVTTL	**EEPROM Serial Data Input** During Samurai-5LC/5LCX (ADM6995LC/LCX) initialization, this pin is used to output address and command to access EEPROM. After the initialization process is done, this pin becomes an input pin to monitor EEPROM data if **IFSEL** = 1.
	SDIO	I/O	8 mA, PD, LVTTL	**Serial Management interface Data input/Output** If **IFSEL** = 0, this pin is used as data input/output pin of serial management interface.
Power/Ground, 48 Pins				
10, 23, 36, 42, 125	GNDA	GND	–	**Ground** Used by AD Block
7, 20, 33, 45, 122	VCCA2	PWR	–	**1.8 V, Power** Used by TX Line Driver
13, 26, 39, 128	VCCAD	PWR	–	**3.3 V, Power** Used by AD Block
119	GNDBIAS	GND	–	**Ground** Used by Bias Block
121	VCCBIAS	PWR	–	**3.3 V, Power** Used by Bias Block.
116	GNDPLL	GND	–	**Ground** Used by PLL
115	VCCPLL	PWR	–	**1.8 V, Power** Used by PLL
47, 52, 64, 76, 83, 93	GNDIK	GND	–	**Ground** Used by Digital Core
48, 53, 65, 75, 82, 94, 110	VCCIK	PWR	–	**1.8 V, Power** Used by Digital Core
46, 57, 69, 70, 87, 99, 104	GNDO	GND	–	**Ground** Used by Digital Pad
56, 71, 88, 105	VCC3O	PWR	–	**3.3 V, Power** Used by Digital Pad
Miscellaneous				

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
63	GFCEN	I	PU, LVTTL	**Global Flow Control Enable** Value on this pin will be latched by Samurai-5LC/5LCX (ADM6995LC/LCX) at the rising edge of RESETL(**RC**) as Flow control enable. *Note: Power On Setting* 0_B Flow Control Capability is dependent upon the register setting in corresponding EEPROM register 1_B All ports flow control capability is enabled
66	PHYAS0	I	PD, LVTTL	**PHY Address MSB Bit 0** During power on reset, value will be latched by Samurai-5LC/5LCX (ADM6995LC/LCX) at the rising edge of RESETL as PHY start address select. PHYAS[1:0] = 00_B and PHY address start from 01000_B *Note: Power On Setting*
62	P4FX	I	PD, LVTTL	**Port 4 Fiber Selection** During power on reset, value will be latched by Samurai-5LC/5LCX (ADM6995LC/LCX) at the rising edge of RESETL as Port 4 Fiber select. 0_B Twisted Pair Mode 1_B Fiber Mode
1, 2, 3, 4, 5, 6, 14, 15, 16, 17, 18, 19, 27, 28, 29, 30, 31, 32, 59, 60, 61, 67, 68, 72, 73, 74, 77, 78, 89, 90, 91, 100, 101, 102	NC	-	-	**Not Connected**
49	TEST	I	PD, LVTTL	**Test Mode** Reserved and should keep 0 under normal operation.
86	CFG0	I	PU, LVTTL	**Configuration 0** Reserved and should keep 0 under normal operation.
40	MDIO	I/O	8 mA, PU, LVTTL	**Management Data** MDIO transfers management data in and out of the device synchronous to MDC.
44	MDC	I	PD, ST	**Management Data Reference Clock** A non-continuous clock input for management usage. Samurai-5LC/5LCX (ADM6995LC/LCX) will use this clock to sample data input on MDIO and drive data onto MDIO according to rising edge of this clock.

Table 3 IO Signals (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
85	CKO25M	O	8 mA, PD, LVTTL	**25MHz Clock Output** Free Running 25 MHz Clock output (Even during power on reset)
112	RC	I	ST	**RC Input For Power On Reset** This pin is sampled by using the 25 MHz free running clock signal which input from **XI** to generate the low-active reset signal, RESETL. See **Chapter 5.3.2 Power On Reset** for the timing requirement.
113	XI	AI	ANA	**25MHz Crystal /Oscillator Input** 25MHz Crystal or Oscillator Input. Variation is limited to +/-50ppm.
114	XO	AO	ANA	**25M Crystal Output** When connected to oscillator, this pin should left unconnected.
120	RTX	AI	ANA	**Constant Voltage Reference** External 1.0 kΩ 1% resistor connection to ground.
118	VREF	AI	ANA	**Analog Reference Voltage** Used by Internal Bias Circuit for voltage reference. External 0.1uF capacitor connection to ground for noise filter.
117	CONTROL	AI/O	ANA	**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator. External 0.1μF capacitor connection to ground for noise filter, even the pin is un-connected.

3 Function Description

3.1 Functional Descriptions

The Samurai-5LC/5LCX (ADM6995LC/LCX) integrates five 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, five complete 10Base-T modules, a 5 port 10/100 switch controller and memory into a single chip for both 10Mbit/s and 100Mbit/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbit/s and 100Mbit/s. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The Samurai-5LC/5LCX (ADM6995LC/LCX) consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in SSRAM

The interfaces used for communication between the PHY block and switch core is an MII interface.

An auto MDIX function is supported in this block. This function can be Enabled and Disabled by the hardware pin.

3.2 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.3 100Base-X Module

The Samurai-5LC/5LCX (ADM6995LC/LCX) implements a 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 2. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100Mbit/s PHY loop back is included for diagnostic purposes.

3.4 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbit/s receive data stream. The Samurai-5LC/5LCX (ADM6995LC/LCX) implements the 100Base-X receiving state machine diagram as given in the ANSI/IEEE Standard 802.3u, Clause 24. The 125 Mbit/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and timing recovery module
- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block

- Symbol Decoder
- Collision Detect Block
- Carrier sense Block
- Stream decoder block

3.4.1 A/D Converter

A high performance A/D converter with a 125 MHz sampling rate converts signals received on the RXP/RXN pins to 6 bits data streams. It possesses an auto-gain-control capability that will further improve receive performance especially under long cabling or harsh detrimental signal integrity. Due to high pass characteristic on a transformer, a built in base-line-wander correcting circuit will be cancelled out and its DC level restored.

3.4.2 Adaptive Equalizer and timing Recovery Module

All digital design is especially immune to noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates for line loss induced from twisted pairs and tracks a far end clock at 125M samples per second. Adaptive Equalizer's implemented with Feed forward and Decision Feedback techniques meet the requirement of BER with less than 10-12 for transmission on a CAT5 twisted pair cable ranging from 0 to 120 meters.

3.4.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to the 4B/5B code group's boundary.

3.4.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 micro second countdown. Upon detection of sufficient idle symbols within the 722 micro sec. period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given an operating network connection operating with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within the 722 micro second period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.4.5 Symbol Alignment

The symbol alignment circuit in the Samurai-5LC/5LCX (ADM6995LC/LCX) determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair ($11000\ 10001_B$) is detected, subsequent data is aligned on a fixed boundary.

3.4.6 Symbol Decoding

The symbol decoder functions is a look-up table that translates incoming 5B symbols into 4B nibbles as shown in Table 1. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with a MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines where RXD[0] represents the least significant bit of the translated nibble.

3.4.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous receive clock, RXCLK. RXDV is asserted when the first nibble of a translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.4.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.4.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The Samurai-5LC/5LCX (ADM6995LC/LCX) performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbit/s link status to form the reportable link status bit in the serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 micro secs, and waits for an enable from the auto negotiation module. When received, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.4.10 Carrier Sense

Carrier sense (CRS) for 100Mbit/s operation is asserted upon the detection of two non contiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.4.11 Bad SSD Detection

A Bad Start of Stream Delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if a carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the Samurai-5LC/5LCX (ADM6995LC/LCX) will assert RXER and present RXD[3:0] = 1110_B to the internal MII for the cycles that correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.4.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station’s transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all 1_B's to a group of 84 1_B's followed by a single 0_B. This is referred to as the FEFI idle pattern.

3.5 100Base-TX Transceiver

The Samurai-5LC/5LCX (ADM6995LC/LCX) implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmissions with a simple RC component connection. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

3.5.1 Transmit Drivers

The Samurai-5LC/5LCX (ADM6995LC/LCX) 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range as specified in the ANSI TP-PMD standard.

3.5.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The Samurai-5LC/5LCX (ADM6995LC/LCX) uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard. Figure 3 provides an overview for the 10Base-T module.

The Samurai-5LC/5LCX (ADM6995LC/LCX) 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.6.1 Operation Modes

The Samurai-5LC/5LCX (ADM6995LC/LCX) 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the Samurai-5LC/5LCX (ADM6995LC/LCX) functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the Samurai-5LC/5LCX (ADM6995LC/LCX) can simultaneously transmit and receive data.

3.6.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in a good link state. Transmission ends when the transmission enable input goes low.

The last transition occurs at the center of the bit cell if the last bit is a 1_B, or at the boundary of the bit cell if the last bit is 0_B.

Decoding is accomplished using a differential input receiver circuit and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and a half bit times after the last bit, carrier sense is de-asserted.

3.6.3 Transmit Driver and Receiver

The Samurai-5LC/5LCX (ADM6995LC/LCX) integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.6.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The Samurai-5LC/5LCX (ADM6995LC/LCX) implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating the end of a packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11_H.

3.7 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbit/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbit/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.8 Jabber Function

The jabber function monitors the Samurai-5LC/5LCX (ADM6995LC/LCX) output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (the un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10_H to high.

3.9 Link Test Function

A link pulse is used to check he integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data.

3.10 Automatic Link Polarity Detection

The Samurai-5LC/5LCX (ADM6995LC/LCX)'s 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10_H.

3.11 Clock Synthesizer

The Samurai-5LC/5LCX (ADM6995LC/LCX) implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.12 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The Samurai-5LC/5LCX (ADM6995LC/LCX) supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority is relative to the following list:

- 100Base-TX full duplex (highest priority)
- 100Base-TX half duplex
- 10Base-T full duplex
- 10Base-T half duplex (lowest priority)

3.13 Memory Block

The Samurai-5LC/5LCX (ADM6995LC/LCX)'s built in memory is divided into two blocks. One is a MAC addressing table and the other one is a data buffer.

The MAC address Learning Table size is 2K entries with each entry occupying eight bytes length. These eight bytes of data include a 6 byte source address, VLAN information, Port information and an aging counter.

A data buffer is divided into 256 bytes/block. The Samurai-5LC/5LCX (ADM6995LC/LCX) buffer management is per port fixed block number and all ports share one global buffer. This architecture can get better memory utilization and network balance at different speeds and duplex test conditions.

Received packets will separate into several 256 bytes/block and chain together. If a packet size is more than 256 bytes then the Samurai-5LC/5LCX (ADM6995LC/LCX) will chain two or more blocks to store receiving packets.

3.14 Switch Functional Description

The Samurai-5LC/5LCX (ADM6995LC/LCX) uses a "store & forward" switching approach for the following reason:

- Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require large elastic buffers especially when bridging between a server on a 100 Mbit/s network and clients on a 10 Mbit/s segment.
- Store & forward switches improve overall network performance by acting as a "network cache"
- Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.15 Basic Operation

The Samurai-5LC/5LCX (ADM6995LC/LCX) receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within the same VLAN group, where appropriate. If the destination address is not found in the address table, the Samurai-5LC/5LCX (ADM6995LC/LCX) treats the packet as a broadcast packet and forwards the packet to the other ports within the same VLAN group.

The Samurai-5LC/5LCX (ADM6995LC/LCX) automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.15.1 Address Learning

A four-way hash algorithm is implemented to allow the maximum of 4 different addresses with the same hash key to be stored at the same time. Up to 2K entries can be created and all entries are stored in the internal SSRAM. An address is stored in the Address Table. The Samurai-5LC/5LCX (ADM6995LC/LCX) searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

1. If the SA was not found in the Address Table (a new address), the Samurai-5LC/5LCX (ADM6995LC/LCX) waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then the aging value of each corresponding entry will be reset to 0_B.
2. When the DA is PAUSE command, then the learning process will be disabled automatically by Samurai-5LC/5LCX (ADM6995LC/LCX).

3.15.2 Address Recognition and Packet Forwarding

The Samurai-5LC/5LCX (ADM6995LC/LCX) forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarded will check the VLAN first. A forwarding port must be the within the same VLAN as the source port.

If the DA is a UNICAST address and the address was found in the Address Table, the Samurai-5LC/5LCX (ADM6995LC/LCX) will check the port number and act as follows:

- If the port number is equal to the port on which the packet was received, the packet is discarded.
- If the port number is different, the packet is forwarded across the bridge.
- If the DA is a UNICAST address and the address was not found, the Samurai-5LC/5LCX (ADM6995LC/LCX) treats it as a multicast packet and forwards it across the bridge.
- If the DA is a Multicast address, the packet is forwarded across the bridge.
- If the DA is a PAUSE Command (01 80 C2 00 00 01_H), then this packet will be dropped by the Samurai-5LC/5LCX (ADM6995LC/LCX). The Samurai-5LC/5LCX (ADM6995LC/LCX) can issue and learn PAUSE commands.
- The Samurai-5LC/5LCX (ADM6995LC/LCX) will forward the packet with a DA of (01 80 C2 00 00 00_H), filter out the packet with a DA of (01 80 C2 00 00 01_H), and forward a packet with a DA of (01-80-C2-00-00-02_H to 01 80 C2 00 00 $0F_H$)

3.15.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to another. When this happens, the Samurai-5LC/5LCX (ADM6995LC/LCX) internally has a 300 second timer which will “age-out” (remove) the address from the address table. The aging function can be enabled/disabled by the user. Normally, disabling an aging function is for security purposes.

3.15.4 Back off Algorithm

The Samurai-5LC/5LCX (ADM6995LC/LCX) implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. The Samurai-5LC/5LCX (ADM6995LC/LCX) will restart the back off algorithm

by choosing 0-9 collision counts. The Samurai-5LC/5LCX (ADM6995LC/LCX) resets the collision counter after 16 consecutive retransmit trials.

3.15.5 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits at a time. The value is 9.6 micro secs for 10 Mbit/s Ethernet, 960ns for 100 Mbit/s fast Ethernet and 96ns for 1000M. The Samurai-5LC/5LCX (ADM6995LC/LCX) provides an option of 92 bit gap in an EEPROM to prevent packet loss when Flow Control is turned off and clock P.P.M. values differ.

3.15.6 Illegal Frames

The Samurai-5LC/5LCX (ADM6995LC/LCX) will discard all illegal frames such as runt packets (less than 64 bytes), oversized packets (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will be accepted by the Samurai-5LC/5LCX (ADM6995LC/LCX). In case of bypass mode enable, the Samurai-5LC/5LCX (ADM6995LC/LCX) will support tag and untagged packets with sizes up to 1522 bytes. In case of non-bypass mode, the Samurai-5LC/5LCX (ADM6995LC/LCX) will support tag packets up to 1526bytes and untagged packets up to 1522bytes.

3.15.7 Half Duplex Flow Control

A back pressure function is supported for half-duplex operations. When the Samurai-5LC/5LCX (ADM6995LC/LCX) cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET assertion. An Infineon proprietary algorithm is implemented inside the Samurai-5LC/5LCX (ADM6995LC/LCX) to prevent the back pressure function causing HUB partitioned under heavy traffic environment and reducing the packet loss rate to increase the whole system performance.

3.15.8 Full Duplex Flow Control

When full duplex port run out of its receive buffer, a PAUSE packet command will be issued by Samurai-5LC/5LCX (ADM6995LC/LCX) to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. Samurai-5LC/5LCX (ADM6995LC/LCX) can issue or receive pause packet.

3.15.9 Broadcast Storm filter

If the Broadcast Storm filter is enabled, the broadcast packets over 50 ms of the threshold will be discarded by the threshold setting. See EEPROM Reg.10_H.

Broadcast storm mode:

Time interval: 50ms

Max. packet number = 7490 in 100Base, 749 in 10Base

Table 4 The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Falling Threshold				
	00_B	01_B	10_B	11_B
All 100TX	Disable	7440fps	14880fps	29760fps
Not All 100TX	Disable	744fps	1488fps	2976fps

Table 5 The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Rising Threshold				
	00_B	01_B	10_B	11_B
All 100TX	Disable	14880fps	29760fps	59520fps
Not All 100TX	Disable	1488fps	2976fps	5952fps

3.16 Auto TP MDIX Function

For normal applications with the Switch connected to a NIC should be done using one TP cable. If the Switch connects to other devices, such as another Switch, it must be by two ways only: Cross Over TP cable and extra RJ45 which crossover internal TX+- and RX+- signal. Using the RJ45 system one by one cable to connect two Switch devices is used. All these efforts require extra cost and are not good solutions. Samurai-5LC/5LCX (ADM6995LC/LCX) provides an Auto MDIX function which can adjust TX+- and RX+- using the correct pin. Users can then use one by one cable between Samurai-5LC/5LCX (ADM6995LC/LCX) and other devices. This function can be Enable/Disabled by hardware pins and EEPROM configuration register 01_H ~ 09_H bit 15. If hardware pins set all ports to Auto MDIX mode then EEPROM setting is useless. If hardware pins set all ports at non Auto MDIX mode then EEPROM can set each port for this function to enable or disable.

3.17 Port Locking

THe Port Locking function provides a simple way to limit per port user numbers to one. If this function is turned on then Samurai-5LC/5LCX (ADM6995LC/LCX) will lock the first MAC address in the learning table. After this MAC address locking it will never age out except after a Reset signal. Another MAC address which is not the same as the locking one will be dropped. Samurai-5LC/5LCX (ADM6995LC/LCX) provides one MAC address per port. This function is per port setting. If Port Locking function is turned on, recommend aging function be turned off. See EEPROM register 12_H bits 0~8.

3.18 VLAN setting & Tag/Untag & port-based VLAN

Samurai-5LC/5LCX (ADM6995LC/LCX) supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without a tag will be forwarded to the destination port without any modification by Samurai-5LC/5LCX (ADM6995LC/LCX). Meanwhile port-based VLAN can be enabled according to the PVID value (user define 4bits to map 16 groups written at register 13_H to register 22_H) of the configuration content of each port.

Samurai-5LC/5LCX (ADM6995LC/LCX) also supports 16 802.1Q VLAN groups. In VLAN four byte tags include twelve VLAN IDs. Samurai-5LC/5LCX (ADM6995LC/LCX) lets user define four bits of VID. If users need to use this function, two EEPROM registers are needed to be programmed first:

* Port VID number at EEPROM register 01_H ~ 09_H bit 13~10, register 28_H ~ $2B_H$ and register $2C_H$ bit 7~0: Samurai-5LC/5LCX (ADM6995LC/LCX) will check coming packet. If coming packet is non VLAN packet then Samurai-5LC/5LCX (ADM6995LC/LCX) will use PVID as VLAN group reference. Samurai-5LC/5LCX (ADM6995LC/LCX) will use packet's VLAN value when receive tagged packet.

* VLAN Group Mapping Register. EEPROM register 13_H ~ 22_H define VLAN grouping value. User use these register to define VLAN group.

User can define each port as a Tag port or Untag port using Configuration register Bit 4. The operation of packets between Tag ports and Untag port can be explained by the follow example:

Example 1: Port receives Untag packet and sends to Untag port.

Samurai-5LC/5LCX (ADM6995LC/LCX) will check the port user defined four bits of VLAN ID first then check VLAN group resister. If destination port is the same VLAN as receiving port then this packet will forward to destination port without any change. If the destination port is not the same VLAN as receiving port then this packet will be dropped.

Example 2: Port receives Untag packet and send to Tag port.

Samurai-5LC/5LCX (ADM6995LC/LCX) will check the port user defined fours bits of VLAN ID first then check VLAN group resister. If destination port is the same VLAN as receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If destination port not same VLAN as receiving port then this packet will be dropped.

Example 3: Port receives Tag packet and send to Untag port.

Samurai-5LC/5LCX (ADM6995LC/LCX) will check the packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port after remove four bytes with new CRC error. If destination port not same VLAN as receiving port then this packet will be dropped.

Example 4: Port receives Tag packet and send to Tag port.

Samurai-5LC/5LCX (ADM6995LC/LCX) will check the user define packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

3.19 Priority Setting

It is a trend that data, voice and video will be put on the network, a Switch not only deals with data packets but also provides service for multimedia data. The Samurai-5LC/5LCX (ADM6995LC/LCX) provides two priority queues on each port with 8:4:2:1 rate. See EEPROM Reg.10_H.

This priority function can be set in three ways as below:

* By Port Base: Set specific port at specific queue. Samurai-5LC/5LCX (ADM6995LC/LCX) only check the port priority and not check packet's content VLAN and TOS.

* By VLAN first: Samurai-5LC/5LCX (ADM6995LC/LCX) checks VLAN three priority bit first then IP TOS priority bits.

* By IP TOS first: Samurai-5LC/5LCX (ADM6995LC/LCX) checks IP TOS three priority bits first then VLAN three priority bits.

If ports are set at VLAN/TOS priority but receive packets without VLAN or TOS information then port based priority will be used.

3.20 LED Display

Three LED per port are provided by Samurai-5LC/5LCX (ADM6995LC/LCX). Link/Act, Duplex/Col. & Speed are three LED display of Samurai-5LC/5LCX (ADM6995LC/LCX). Dual color LED mode is also supported by Samurai-5LC/5LCX (ADM6995LC/LCX). For easy production purposes Samurai-5LC/5LCX (ADM6995LC/LCX) will send test signal to each LED at power on reset stage. EEPROM register 12_H defines the LED configuration table.

1. **LED_MODE**: It is the value latched on the EDI pin during the power on reset. It's also used to control the dual or single color mode and is useless when the value wait_init is high.
2. **DCS** (see 0012H): Dupcol LEDs indicates the duplex status only.
3. **DHCOL** (See 0030H): When enabled, pin DUPCOL0 shows col_10m status and pin DUPCOL1 shows col_100m status. These two LEDs are necessary in the dual-speed hub.

Samurai-5LC/5LCX (ADM6995LC/LCX) LED is active Low signal. Dupcol0 & Dupcol1 will check external signals at Reset time. If external signals add pull high then LED will be active Low. If external signals add pull down resister then LED will drive high.

3.20.1 Single Color LED Display

Table 6 Single Color LED Display

Pin Name	Status
LNKACT4/LNKACT3/ LNKACT2/LNKACT1/ LNKACT0	These pins have no power on reset values on them, and ADM6995LC/LCX uses active low value to drive the led. So the output values of these pins after the power on reset are shown as follows: 1. First period: This period lasts 1.28 s for LED on test. Samurai-5LC/5LCX (ADM6995LC/LCX) drives value 0 to open the LED. 2. Second period: This period lasts 0.48 s for LED off test. Samurai-5LC/5LCX (ADM6995LC/LCX) drives value 1 to close the LED. 3. Normal Period: Tis period indicates the link status. 0B Port links up and LED is ON. 1B Port links down and LED is OFF. 0/1B Port links up and is transmitting or receiving. The LED flashes at 10 Hz.
LDSPD4/LDSPD3/ LDSPD2/LDSPD1/ LDSPD0	The behavior of these pins is the same as the LNKACT, except during a normal period. Normal period: This period indicates the speed status. 0B Port links up and its speed is 100M. LED is ON. 1B Port links down or its speed is 10M. LED is OFF.

Table 6 Single Color LED Display (cont'd)

Pin Name	Status
DUPCOL2/ DUPCOL1/ DUPCOL0	These 3 pins have power on reset values on them. Samurai-5LC/5LCX (ADM6995LC/LCX) needs to consider these values to drive the correct value. If the power on reset value is value_power_on, then the display is as follows: 1. First period: This period lasts 1.28 s for LED on test. Samurai-5LC/5LCX (ADM6995LC/LCX) drives ~value_power_on to open the LED. 2. Second period: This period lasts 0.48 s for LED off test. Samurai-5LC/5LCX (ADM6995LC/LCX) drives value_power_on to close the LED. 3. Normal Period: Tis period indicates the duplex/collision status. ~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED flashes at 10 Hz. 0/1B Port links up and collision is detected. The LED flashes at 10 Hz. If **DCS** is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1B This value is cancelled. LED doesn't blink. If **DHCOL** is enabled, the display in the normal period is as follows: DUPCOL0: 10m collision indicator. 0/1B One of the ports links up in 10M half-duplex mode and detects a collision event. The LED flashes at 20 Hz. value_power_on = When the above event is not satisfied, the LED is OFF. DUPCOL1: 100 m collision indicator. 0/1B One of the ports links up in 100M half-duplex mode and detects a collision event. The LED flashes at 20 Hz. value_power_on = The above event is not satisfied. LED is OFF.
DUPCOL4/ DUPCOL3	The behavior of these pins is the same as the LNKACT, except the normal period. Normal period: This period indicates the duplex/collision status. ~value_power_on = Port links up in the full-duplex mode. LED is ON. value_power_on = Port links down. LED is OFF. 0/1B Port links up and collision is detected. The LED flashes at 10 Hz. If **DCS** is enabled, the normal period changes its way to display. ~value_power_on = Port links up in the duplex mode. LED is ON. value_power_on = Port links down or links up in the half-duplex mode. LED is OFF. 0/1B This value is cancelled. LED doesn't blink.

3.20.2 Dual Color LED Display

Users should be careful that DUPCOL LED only supports the single color mode. The only difference between single and dual color for DUPCOL LED is during the self-test time.

Table 7 Dual Color LED Display

Pin Name	Status
(LNKACT4, LDSPD4)/ (LNKACT3, LDSPD3) (LNKACT2, LDSPD2) (LNKACT1, LDSPD1) (LNKACT0, LDSPD0)	First Period: Test LED on with green color. It lasts 1.28 s. 01B LED is on with green color. Second Period: Test LED on with yellow color. It lasts 1.28 s. 10B LED is on with yellow color. Third period: Test LED off. 00B LED is off. Normal Period: This period shows the status of the link and speed at the same time. 00B Port links down.LED is off. 11B Port links down. LED is off. 01B Port links up in 100M. LED glows green. 10B Port links up in 10M. LED glows yellow. 0/1,1B Port links up in 100M and is receiving or transmitting. LED blinks with green color at 10 Hz. 0/1,0B Port links up in 10M and is receiving or transmitting. LED blinks with yellow color at 10 Hz.
DUPCOL4/DUPCOL3/ DUPCOL2/DUPCOL1/ DUPCOL0	The behavior of these pins is the same as the single mode, except the self-test period. The LED on test period is 2.56 s instead of 1.28 s.

3.20.3 Circuit for Single LED Mode

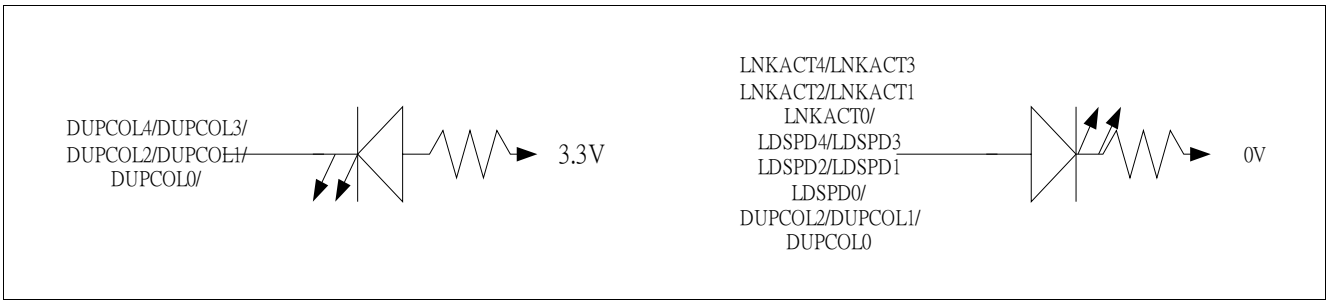


Figure 3 Circuit for Single Color LED Mode

3.20.4 Circuit for Dual Led Mode

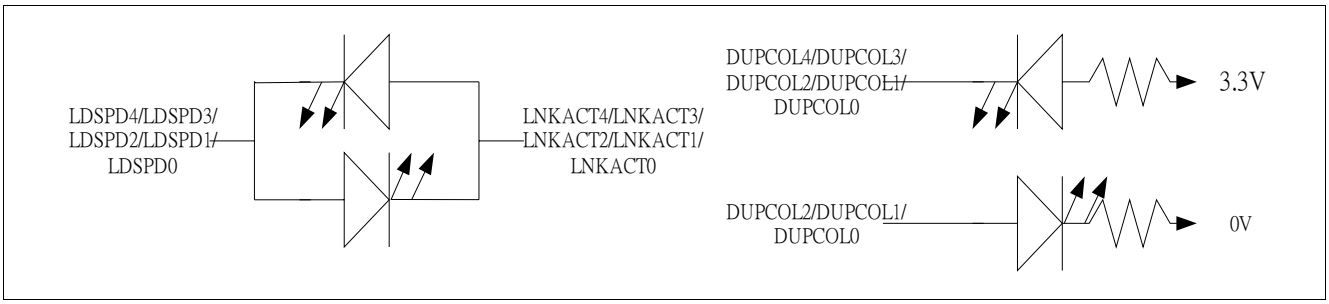


Figure 4 Circuit for Dual Color LED Mode

4 Registers Description

4.1 EEPROM Registers

Table 8 Registers Address Space

Module	Base Address	End Address	Note
EEPROM	00_H	33_H	Independent Address Space

Table 9 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SigReg	Signature Register	00_H	33
CtrlReg_0	Basic Control Register 0	01_H	34
ResReg_0	Reserved Register 0	02_H	35
CtrlReg_P1	Basic Control Register 1	03_H	35
ResReg_1	Reserved Register 1	04_H	36
CtrlReg_P2	Basic Control Register 2	05_H	35
ResReg_2	Reserved Register 2	06_H	36
CtrlReg_P3	Basic Control Register 3	07_H	35
CtrlReg_P4	Basic Control Register 4	08_H	35
ResReg_3	Reserved Register 3	09_H	36
ResReg_4	Reserved Register 4	$0A_H$	36
ConfigReg_1	Configuration Register 1	$0B_H$	36
ResReg_5	Reserved Register 5	$0C_H$	36
ResReg_6	Reserved Register 6	$0D_H$	36
VLAN_Map_P	VLAN priority Map Register	$0E_H$	37
TOS_Priority	TOS priority Map Register	$0F_H$	38
ConfigReg_2	Configuration Register 2	10_H	38
ConfigReg_3	Miscellaneous Configuration Register 3	12_H	39
VLAN_Map_0	VLAN mapping table registers 0	13_H	40
VLAN_Map_1	VLAN mapping table registers 1	14_H	41
VLAN_Map_2	VLAN mapping table registers 2	15_H	41
VLAN_Map_3	VLAN mapping table registers 3	16_H	41
VLAN_Map_4	VLAN mapping table registers 4	17_H	41
VLAN_Map_5	VLAN mapping table registers 5	18_H	41
VLAN_Map_6	VLAN mapping table registers 6	19_H	41
VLAN_Map_7	VLAN mapping table registers 7	$1A_H$	41
VLAN_Map_8	VLAN mapping table registers 8	$1B_H$	41
VLAN_Map_9	VLAN mapping table registers 9	$1C_H$	41
VLAN_Map_10	VLAN mapping table registers 10	$1D_H$	41
VLAN_Map_11	VLAN mapping table registers 11	$1E_H$	41

Table 9 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
VLAN_Map_12	VLAN mapping table registers 12	$1F_H$	41
VLAN_Map_13	VLAN mapping table registers 13	20_H	41
VLAN_Map_14	VLAN mapping table registers 14	21_H	42
VLAN_Map_15	VLAN mapping table registers 15	22_H	42
ResReg_7	Reserved Register 7	23_H	36
ResReg_8	Reserved Register 8	24_H	36
ResReg_9	Reserved Register 9	25_H	36
ResReg_10	Reserved Register 10	26_H	36
ResReg_11	Reserved Register 11	27_H	36
ConfigReg_4	Configuration Register 4	28_H	42
ConfigReg_5	Configuration Register 5	29_H	42
ConfigReg_6	Configuration Register 6	$2A_H$	42
ConfigReg_7	Configuration Register 7	$2B_H$	43
ConfigReg_8	Configuration Register	$2C_H$	43
ResReg_12	Reserved Register 12	$2D_H$	36
ResReg_13	Reserved Register 13	$2E_H$	36
PH_Restart	PHY Restart	$2F_H$	44
ConfigReg_	Miscellaneous Configuration Register 9	30_H	45
BWCon_0	Bandwidth Control Register 0	31_H	45
BWCon_1	Bandwidth Control Register 1	32_H	46
BWConEn	Bandwidth Control Enable Register	33_H	47

The register is addressed wordwise.

Table 10 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)

Table 10 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 11 Registers Clock Domains

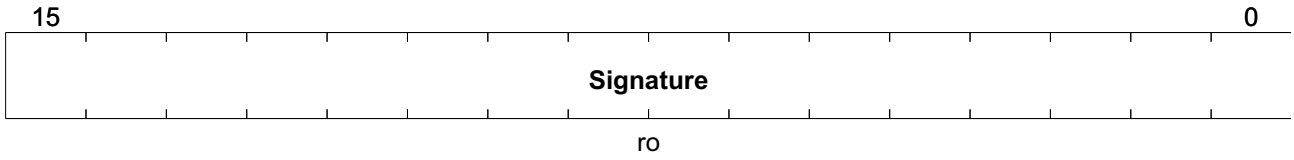
Clock Short Name	Description
–	–

4.1.1 EEPROM Register Descriptions

Signature Register

Description

SigReg	Offset	Reset Value
Signature Register	**00_H**	**4154_H**



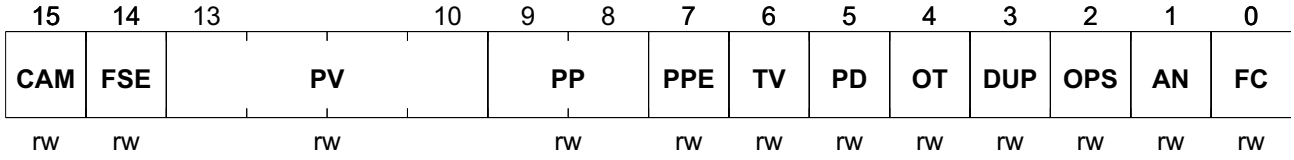
Field	Bits	Type	Description
Signature	15:0	ro	**Signature** 4154_H **SigReg** Obligatory value (AT)

Note: Samurai-5LC/5LCX (ADM6995LC/LCX) will check register 0 value before reading all EEPROM content. If this value does not match with 0x4154h then other values in EEPROM will be useless. Samurai-5LC/5LCX (ADM6995LC/LCX) will use internal default value. User cannot write Signature register when programming Samurai-5LC/5LCX (ADM6995LC/LCX) internal register.

Basic Control Register 0

Used to configure chip settings

CtrlReg_0	Offset	Reset Value
Basic Control Register 0	**01_H**	**$040F_H$**



Field	Bits	Type	Description
CAM	15	rw	**Crossover Auto MDIX** 0_B **D** Disable *Note: Hardware Reset latch value EESK can be set globally using the Auto MDIX function.* 1_B **E** Enable
FSE	14	rw	**Fx Select Enable** 0_B **TP** Tp Mode *Note: If this bit has been set to Fx in hardware then the bit does not have the power to change from Fx to Tp* 1_B **FX** Fx Mode
PV	13 :10	rw	**Port VLAN ID**
PP	9:8	rw	**Port Based Priority**
PPE	7	rw	**Port Based Priority Enable** 0_B **VTE** VLAN or TOS Priority Enable *Note: This bit is default 0_B to enable VLAN or TOS priority check. If user would like to check the VLAN priority, Tag mode should be enabled.* 1_B **PBE** Port Based Priority Enable *Note: If this bit is set to 1_B, only port based priority will be checked.*
TV	6	rw	**TOS over VLAN priority** Enable checking TOS priority first then VLAN priority if both priority happen on coming packet. 0_B **V** VLAN Enable 1_B **T** TOS Enable
PD	5	rw	**Port Disable** 0_B **E** Enable 1_B **D** Disable

Field	Bits	Type	Description
OT	4	rw	**Output Packet Tagging** 0_B **U** Un-tag 1_B **T** Tag
DUP	3	rw	**Duplex Enable** 0_B **H** Half 1_B **F** Full
OPS	2	rw	**Operating Speed** 0_B **10** 10 Mbit/s 1_B **100** 100 Mbit/s
AN	1	rw	**Auto-negotiation** 0_B **D** Disable 1_B **E** Enable
FC	0	rw	**802.x Flow Control Command** 0_B **D** Disable 1_B **E** Enable

Similar Registers

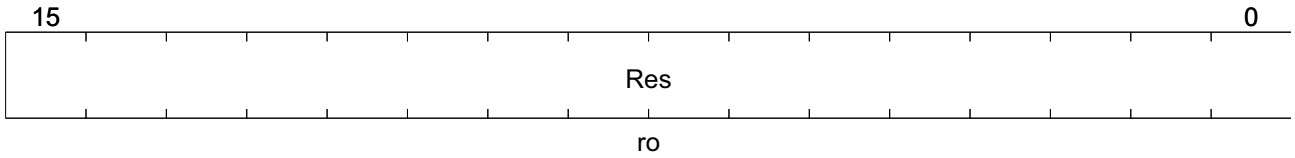
Table 12 Basic Control Registers 1 to 4

Register Short Name	Register Long Name	Offset Address	Page Number
CtrlReg_P1	Basic Control Register 1	03_H	
CtrlReg_P2	Basic Control Register 2	05_H	
CtrlReg_P3	Basic Control Register 3	07_H	
CtrlReg_P4	Basic Control Register 4	08_H	

Reserved Register 0

Register reserved for future use

ResReg_0	Offset	Reset Value
Reserved Register 0	**02_H**	**$040F_H$**



Field	Bits	Type	Description
Res	15:0	ro	**Reserved**

Similar Registers

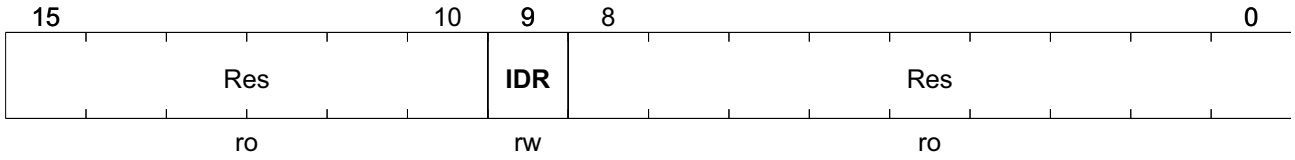
Table 13 Reserved Register 1 to 3

Register Short Name	Register Long Name	Offset Address	Page Number
ResReg_1	Reserved Register 1	04_H	
ResReg_2	Reserved Register 2	06_H	
ResReg_3	Reserved Register 3	09_H	
ResReg_5	Reserved Register 5	$0C_H$	
ResReg_6	Reserved Register 6	$0D_H$	
ResReg_7	Reserved Register 7	23_H	
ResReg_8	Reserved Register 8	24_H	
ResReg_9	Reserved Register 9	25_H	
ResReg_10	Reserved Register 10	26_H	
ResReg_11	Reserved Register 11	27_H	
ResReg_12	Reserved Register 12	$2D_H$	
ResReg_13	Reserved Register 13	$2E_H$	

Reserved Register 4

Register reserved for future use

ResReg_4	Offset	Reset Value
Reserved Register 4	**$0A_H$**	**5902_H**

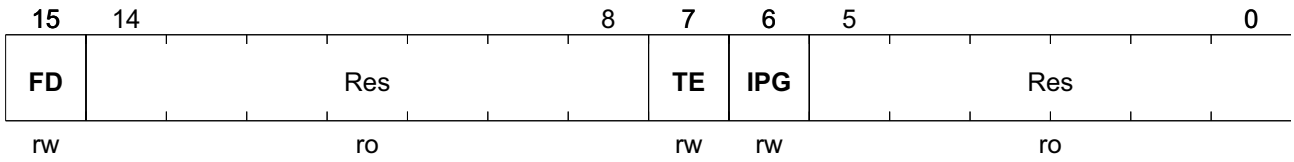


Field	Bits	Type	Description
Res	15:10	ro	**Reserved**
IDR	9	rw	**Replace Packet ID** 0_B **N** Not replaced 1_B **Y** Replaced with 1 by PVID
Res	8:0	ro	**Reserved**

Configuration Register 1

Used to configure the chip

ConfigReg_1	Offset	Reset Value
Configuration Register 1	**$0B_H$**	**8000_H**

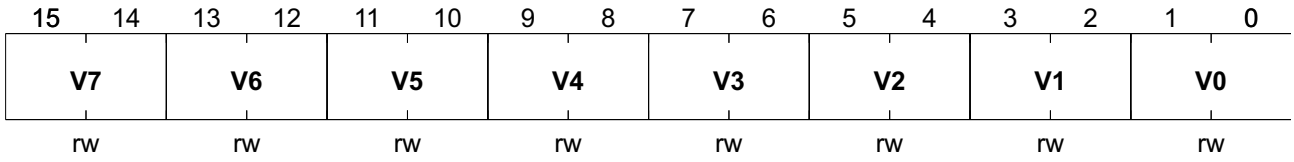


Field	Bits	Type	Description
FD	15	rw	**Far End Fault Detection** 0_B **D** Disable 1_B **E** Enable
Res	14:8	ro	**Reserved**
TE	7	rw	**Trunk Enable** 0_B **D** Disable Port 3 and 4 1_B **E** Enable Port 3 and 4
IPG	6	rw	**Inter Packet Gap Setting** 0_B **96B** 96 bits 1_B **92B** 92 bits
Res	5:0	ro	**Reserved**

VLAN Priority Map Register

Sets the VLAN priorities

VLAN_Map_P	Offset	Reset Value
VLAN priority Map Register	$0E_H$	5500_H



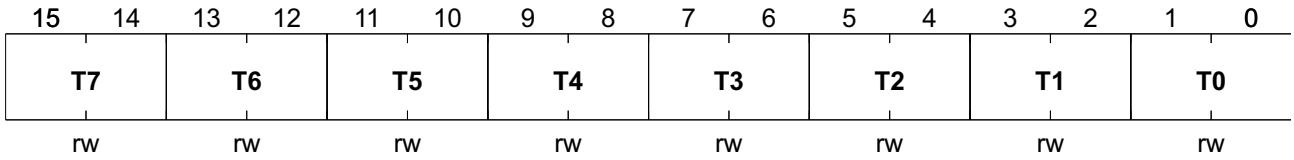
Field	Bits	Type	Description
V7	15:14	rw	**Mapped priority of tag value (VLAN)**
V6	13:12	rw	
V5	11:10	rw	
V4	9:8	rw	
V3	7:6	rw	
V2	5:4	rw	
V1	3:2	rw	
V0	1:0	rw	

Note: Value 3 ~ 0 are for priority queue Q3~Q0 respectively.The Weight ratio is Q3: Q2: Q1: Q0 = 8: 4: 2: 1. The default is port-base priority for un-tagged packets and non_IP frame.

Type of Service (TOS) Priority Map Register

Sets TOS priority

TOS_Priority	Offset	Reset Value
TOS priority Map Register	$0F_H$	5500_H



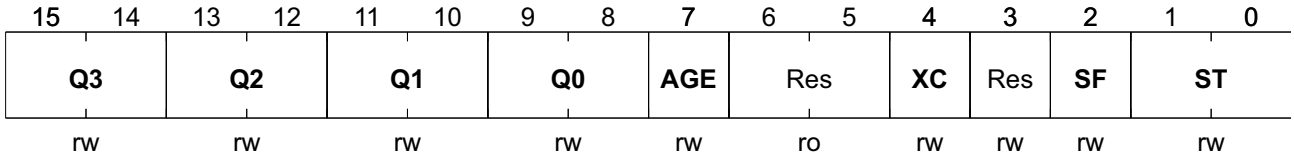
Field	Bits	Type	Description
T7	15:14	rw	**Mapped priority of tag value (TOS)**
T6	13:12	rw	
T5	11:10	rw	
T4	9:8	rw	
T3	7:6	rw	
T2	5:4	rw	
T1	3:2	rw	
T0	1:0	rw	

Note: Value 3 ~ 0 are for priority queues Q3~Q0 respectively. The Weight ratio is Q3: Q2: Q1: Q0 = 8: 4: 2: 1. The default is port-based priority for un-tagged packets and non_IP frames.

Configuration Register 2

Used to configure the chip

ConfigReg_2	Offset	Reset Value
Configuration Register 2	10_H	0040_H



Field	Bits	Type	Description
Q3	15:14	rw	**Discard mode** Drop scheme for Queue n. See **Table 16** for details on the drop scheme of each queue
Q2	13:12	rw	
Q1	11:10	rw	
Q0	9:8	rw	

Field	Bits	Type	Description
AGE	7	rw	**Aging Status** 0_B **E** Enable 1_B **D** Disable
Res	6:5	ro	**Reserved**
XC	4	rw	**CRC Check** 0_B **E** Enable CRC check 1_B **D** Disable CRC check
Res	3	rw	**Reserved**
SF	2	rw	**Broadcast Storm Filter** 0_B **D** Disable 1_B **E** Enable
ST	1:0	rw	**Broadcast Storm Threshold** See below **Table 14** and **Table 15** for details on the Broadcast Storm Threshold

Note: Broadcast storm initial time interval = 50ms. The max. packet number = 7490 in 100Base, 749 in 10Base

Table 14 The max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Rising Threshold				
	00_B	01_B	10_B	11_B
All 100TX	Disable	14880fps	29760fps	59520fps
Not All 100TX	Disable	1488fps	2976fps	5952fps

Table 15 The max. packet number = 7490 in 100Base, 749 in 10Base

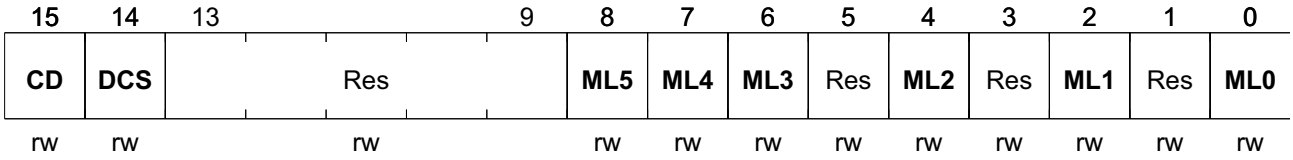
Per Port Falling Threshold				
	00_B	01_B	10_B	11_B
All 100TX	Disable	7440fps	14880fps	29760fps
Not All 100TX	Disable	744fps	1488fps	2976fps

Table 16 Drop Scheme for Each Queue

Discard Mode Utilization	**00**	**01**	**10**	**11**
TBD	0%	0%	25%	50%

Configuration Register 3

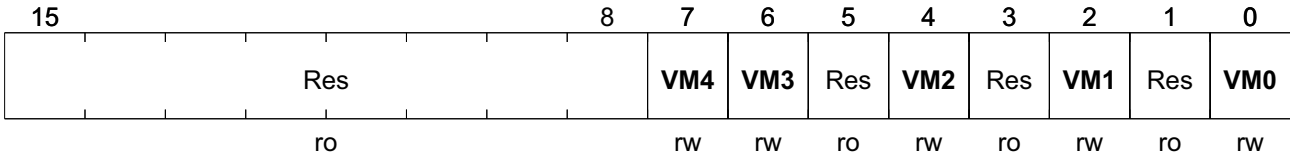
ConfigReg_3	**Offset**	**Reset Value**
Miscellaneous Configuration Register 3	**12_H**	**3600_H**



Field	Bits	Type	Description
CD	15	rw	**Excessive Collision Drop** 0_B **D** Disable 1_B **E** Enable
DCS	14	rw	**Duplex and Col Separate** 0_B **D** Indicate the duplex and collision status at the same time 1_B **LM** Indicate the duplex status only
Res	13:9	rw	**Reserved**
ML5	8	rw	**Port5 MAC Lock** 0_B **D** Disable 1_B **LM** Lock first MAC Source Address
ML4	7	rw	**Port4 MAC Lock** 0_B **D** Disable 1_B **LM** Lock first MAC Source Address
ML3	6	rw	**Port3 MAC Lock** 0_B **D** Disable 1_B **LM** Lock first MAC Source Address
Res	5	rw	**Reserved**
ML2	4	rw	**Port 2 MAC Lock** 0_B **D** Disable 1_B **LM** Lock first MAC source address
Res	3	rw	**Reserved**
ML1	2	rw	**Port1 MAC Lock** 0_B **D** Disable 1_B **LM** Lock first MAC source address
Res	1	rw	**Reserved**
ML0	0	rw	**Port0 MAC Lock** 0_B **D** Disable 1_B **LM** Lock first MAC source address

VLAN Mapping Table Registers 0

VLAN_Map_0	**Offset**	**Reset Value**
VLAN mapping table registers 0	**13_H**	**$FFFF_H$**



Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
VM4	7	rw	**Port 4 VLAN Mapping** 0_B **NM** Port 5 is not the member of the VLAN. 1_B **M** Port 5 is the member of the VLAN.
VM3	6	rw	**Port 3 VLAN Mapping** 0_B **NM** Port 3 is not the member of the VLAN. 1_B **M** Port 3 is the member of the VLAN.
Res	5	ro	**Reserved**
VM2	4	rw	**Port 2 VLAN Mapping** 0_B **NM** Port 2 is not the member of the VLAN. 1_B **M** Port 2 is the member of the VLAN.
Res	3	ro	**Reserved**
VM1	2	rw	**Port 1 VLAN Mapping** 0_B **NM** Port 1 is not the member of the VLAN. 1_B **M** Port 1 is the member of the VLAN.
Res	1	ro	**Reserved**
VM0	0	rw	**Port 0 VLAN Mapping** 0_B **NM** Port 0 is not the member of the VLAN. 1_B **M** Port 0 is the member of the VLAN.

Similar Registers

Table 17 VLAN Mapping Table Registers 1 to 15

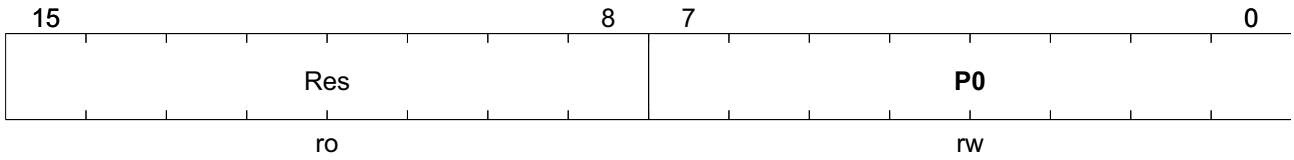
Register Short Name	Register Long Name	Offset Address	Page Number
VLAN_Map_1	VLAN mapping table registers 1	14_H	
VLAN_Map_2	VLAN mapping table registers 2	15_H	
VLAN_Map_3	VLAN mapping table registers 3	16_H	
VLAN_Map_4	VLAN mapping table registers 4	17_H	
VLAN_Map_5	VLAN mapping table registers 5	18_H	
VLAN_Map_6	VLAN mapping table registers 6	19_H	
VLAN_Map_7	VLAN mapping table registers 7	$1A_H$	
VLAN_Map_8	VLAN mapping table registers 8	$1B_H$	
VLAN_Map_9	VLAN mapping table registers 9	$1C_H$	
VLAN_Map_10	VLAN mapping table registers 10	$1D_H$	
VLAN_Map_11	VLAN mapping table registers 11	$1E_H$	
VLAN_Map_12	VLAN mapping table registers 12	$1F_H$	
VLAN_Map_13	VLAN mapping table registers 13	20_H	

Table 17 VLAN Mapping Table Registers 1 to 15 (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
VLAN_Map_14	VLAN mapping table registers 14	21_H	
VLAN_Map_15	VLAN mapping table registers 15	22_H	

Configuration Register 4

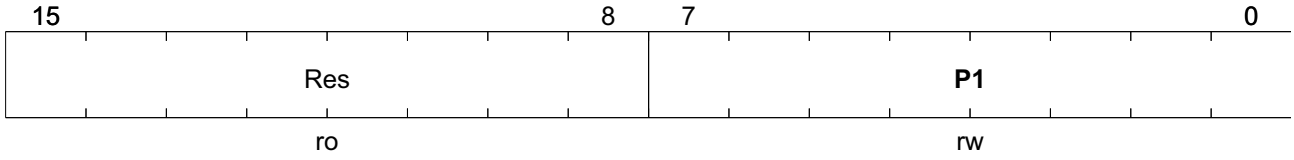
ConfigReg_4	Offset	Reset Value
Configuration Register 4	**28_H**	**0000_H**



Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
P0	7:0	rw	**Port 0 PVID** 0001_H **PVID** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 5

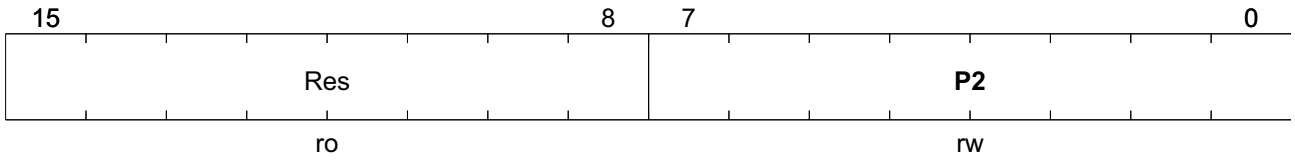
ConfigReg_5	Offset	Reset Value
Configuration Register 5	**29_H**	**0000_H**



Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
P1	7:0	rw	**Port1 PVID bit 11~4.** 0003_H **PVID 1** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 6

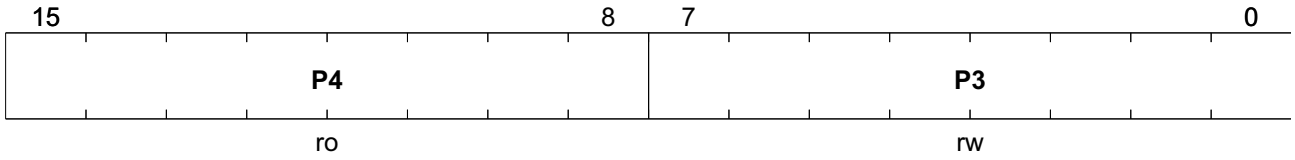
ConfigReg_6	Offset	Reset Value
Configuration Register 6	**$2A_H$**	**0000_H**



Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
P2	7:0	rw	**Port2 PVID bit 11~4.** 0005_H **PVID 2** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 7

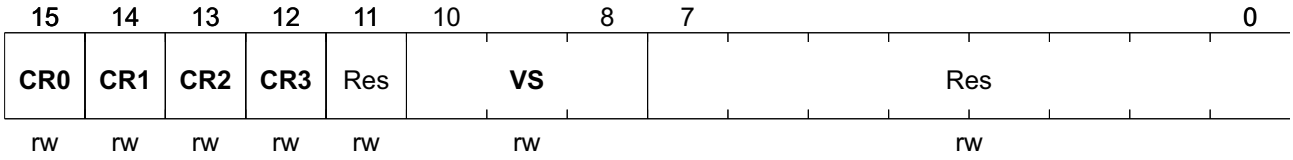
ConfigReg_7	Offset	Reset Value
Configuration Register 7	**$2B_H$**	**0000_H**



Field	Bits	Type	Description
P4	15:8	ro	**Port4 PVID bit 11~4.** 0008_H **PVID 1** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.
P3	7:0	rw	**Port3 PVID bit 11~4.** 0007_H **PVID 1** These 8 bits combine with the register in the hex values bit's [13~10] as the full 12 bits of the VID.

Configuration Register 8

ConfigReg_8	Offset	Reset Value
Configuration Register	**$2C_H$**	**$D000_H$**

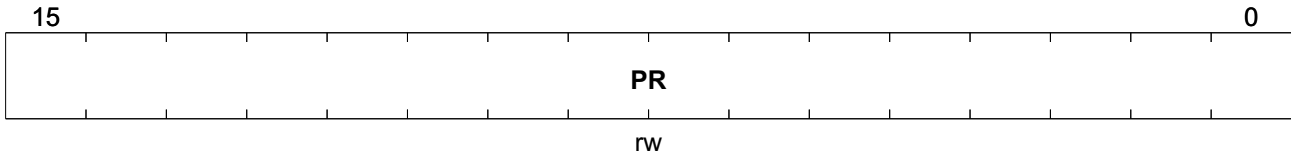


Field	Bits	Type	Description
CR0	15	rw	**Control Reserved MAC** Control reserved MAC (0180C2000000) 0_B **D** Discard 1_B **F** Forward
CR1	14	rw	**Control Reserved MAC** Control reserved MAC (0180C2000001) 0_B **D** Discard 1_B **F** Forward
CR2	13	rw	**Control Reserved MAC** Control reserved MAC (0180C2000002- 0180C200000F) 0_B **D** Discard 1_B **F** Forward
CR3	12	rw	**Control Reserved MAC** Control reserved MAC (0180C2000010-0180C20000FF) 0_B **D** Discard 1_B **F** Forward
Res	11	rw	**Reserved**
VS	10:8	rw	**VLAN Grouping Tag Shift** 0_D **VID0** VID [3:0] 1_D **VID1** VID [4:1] 2_D **VID2** VID [5:2] 3_D **VID3** VID [6:3] 4_D **VID4** VID [7:4] 5_D **VID5** VID [8:5] 6_D **VID6** VID [9:6] 7_D **VID7** VID [10:7]
Res	7:0	rw	**Reserved**

Note: Bit[10:8]: VLAN Tag shift register. Samurai-5LC/5LCX (ADM6995LC/LCX) will select 4 bit form total 12 bit VID as VLAN group reference. Bit[15:12]: IEEE 802.3 reserved DA forward or drop police.

PHY Restart

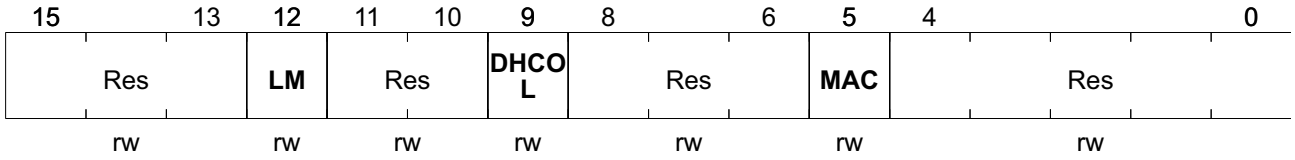
PH_Restart	Offset	Reset Value
PHY Restart	$2F_H$	0000_H



Field	Bits	Type	Description
PR	15:0	rw	**PHY Restart** 0000_H **PHY Restart** Writing this Hex value to this register restarts the internal PHYs.

Configuration Register 9

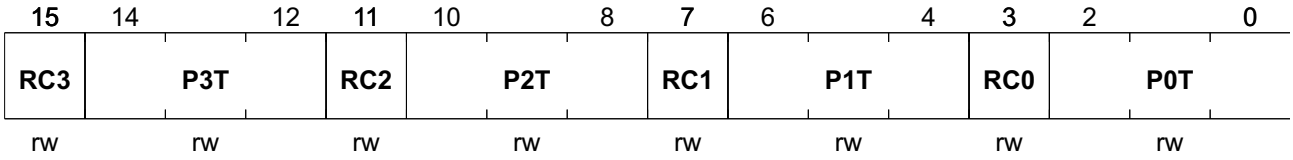
ConfigReg_	Offset	Reset Value
Miscellaneous Configuration Register 9	**30_H**	**0987_H**



Field	Bits	Type	Description
Res	15:13	rw	**Reserved**
LM	12	rw	**Port 4 LED Mode** 0_B **D** LinkAct/DupCol/Speed 1_B **S** LinkAct/Speed
Res	11:10	rw	**Reserved**
DHCOL	9	rw	**Dual Speed Hub COL_LED Enable** 0_B **N** Normal LED display. 1_B **D** Dual Speed Hub LED display. Port0 Col LED: 10M Col LED. Port1 Col LED: 100M Col LED.
Res	8:6	rw	**Reserved**
MAC	5	rw	**Mac Clone Enable** MAC Clone Enable Bit[1].
Res	4:0	rw	**Reserved**

Bandwidth Control Register

BWCon_0	Offset	Reset Value
Bandwidth Control Register 0	**31_H**	**0000_H**



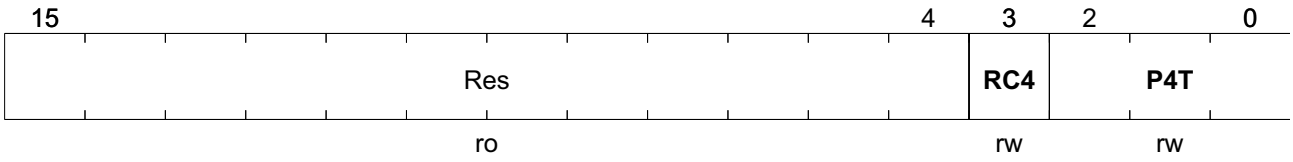
Field	Bits	Type	Description
RC3	15	rw	**Receive Packet Length Count** Counted on the Source Port 3. 0_D **R3** The switch will add length to the P3 counter
P3T	14:12	rw	**Port 3 Threshold Control Meter** Reference **Table 18** in note below.
RC2	11	rw	**Receive Packet Length Count** Counted on the Source Port 2. 0_D **R2** The switch will add length to the P2 counter
P2T	10:8	rw	**Port 2 Threshold Control Meter** Reference **Table 18** in note below.
RC1	7	rw	**Receive Packet Length Count** Counted on the Source Port 1. 0_D **R1** The switch will add length to the P1 counter
P1T	6:4	rw	**Port 1 Threshold Control Meter** Reference **Table 18** in note below.
RC0	3	rw	**Receive Packet Length Count** Counted on the Source Port 0. 0_D **R0** The switch will add length to the P2 counter
P0T	2:0	rw	**Port 0 Threshold Control Meter** Reference **Table 18** in note below.

Table 18 Note:Reference Table

000	001	010	011	100	101	110	111
256K	512K	1M	2M	5M	10M	20M	50M

Bandwidth Control Register 1

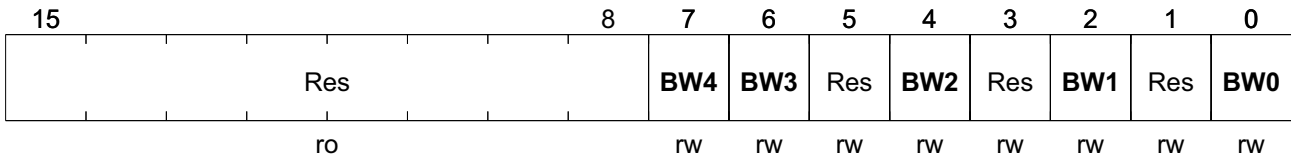
BWCon_1	Offset	Reset Value
Bandwidth Control Register 1	**32_H**	**0000_H**



Field	Bits	Type	Description
Res	15:4	ro	**Reserved**
RC4	3	rw	**Receive Packet Length Count** Counted on the Source Port 4. 0_D **Count4** The switch will add length to the P4 counter
P4T	2:0	rw	**Port 4 Threshold Control Meter** Reference **Table 18** in note below.

Bandwidth Control Enable Register

BWConEn	Offset	Reset Value
Bandwidth Control Enable Register	**33_H**	**0000_H**



Field	Bits	Type	Description
Res	15:8	ro	**Reserved**
BW4	7	rw	**Port 4 Bandwidth Control Enable** 0_B **D** Disable 1_B **E** Enable
BW3	6	rw	**Port 3 Bandwidth Control Enable** 0_B **D** Disable 1_B **E** Enable
Res	5	rw	**Reserved**
BW2	4	rw	**Port 2 Bandwidth Control Enable** 0_B **D** Disable 1_B **E** Enable
Res	3	rw	**Reserved**
BW1	2	rw	**Port 1 Bandwidth Control Enable** 0_B **D** Disable 1_B **E** Enable
Res	1	rw	**Reserved**
BW0	0	rw	**Port 0 Bandwidth Control Enable** 0_B **D** Disable 1_B **E** Enable

4.2 Serial Registers

Table 19 Registers Address Space

Module	Base Address	End Address	Note
Serial Registers	00_H	$3C_H$	Independent Address Space

Table 20 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
ChipID	Chip Identifier Register	00_H	49
PortStat_0	Port Status Register 0	01_H	49
PortStat_1	Port Status Register 1	02_H	51
CabStat	Cable Broken Status	03_H	52
P0_RP_CNT	Port 0 Receive Packet Count	04_H	52
P1_RP_CNT	Port 1 Receive Packet Count	06_H	53
P2_RP_CNT	Port 2 Receive Packet Count	08_H	53
P3_RP_CNT	Port 3 Receive Packet Count	$0A_H$	53
P4_RP_CNT	Port 4 Receive Packet Count	$0B_H$	53
P5_RP_CNT	Port 5 Receive Packet Count	$0C_H$	53
P0_RB_CNT	Port 0 Receive Byte Count	$0D_H$	53
P1_RB_CNT	Port 1 Receive Byte Count	$0F_H$	53
P2_RB_CNT	Port 2 Receive Byte Count	11_H	53
P3_RB_CNT	Port 3 Receive Byte Count	13_H	53
P4_RB_CNT	Port 4 Receive Byte Count	14_H	53
P5_RB_CNT	Port 5 Receive Byte Count	15_H	53
P0_TP_CNT	Port 0 Transmit Packet Count	16_H	53
P1_TP_CNT	Port 1 Transmit Packet Count	18_H	53
P2_TP_CNT	Port 2 Transmit Packet Count	$1A_H$	53
P3_TP_CNT	Port 3 Transmit Packet Count	$1C_H$	53
P4_TP_CNT	Port 4 Transmit Packet Count	$1D_H$	53
P5_TP_CNT	Port 5 Transmit Packet Count	$1E_H$	53
P0_TB_CNT	Port 0 Transmit Byte Count	$1F_H$	53
P1_TB_CNT	Port 1 Transmit Byte Count	21_H	53
P2_TB_CNT	Port 2 Transmit Byte Count	23_H	53
P3_TB_CNT	Port 3 Transmit Byte Count	25_H	53
P4_TB_CNT	Port 4 Transmit Byte Count	26_H	53
P5_TB_CNT	Port 5 Transmit Byte Count	27_H	53
P0_COL_CNT	Port 0 Collision Count	28_H	53
P1_COL_CNT	Port 1 Collision Count	$2A_H$	53
P2_COL_CNT	Port 2 Collision Count	$2C_H$	53
P3_COL_CNT	Port 3 Collision Count	$2E_H$	53
P4_COL_CNT	Port 4 Collision Count	$2F_H$	53
P5_COL_CNT	Port 5 Collision Count	30_H	53

Table 20 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
P0_ERR_CNT	Port 0 Error Count	31_H	53
P1_ERR_CNT	Port 1 Error Count	33_H	53
P2_ERR_CNT	Port 2 Error Count	35_H	53
P3_ERR_CNT	Port 3 Error Count	37_H	53
P4_ERR_CNT	Port 4 Error Count	38_H	53
P5_ERR_CNT	Port 5 Error Count	39_H	53
OverFlow_0	Over Flow Flag Register 0	$3A_H$	53
OverFlow_1	Over Flow Flag Register 1	$3B_H$	54
OverFlow_2	Over Flow Flag Register 2	$3C_H$	55

The register is addressed wordwise.

For Register Access Types please refer to Table 10 "Register Access Types" on Page 32.

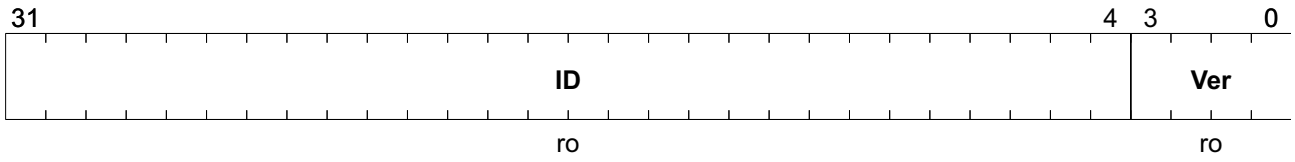
Table 21 Registers Clock Domains

Clock Short Name	Description
–	–

4.2.1 Serial Register Map

Chip Identifier Register

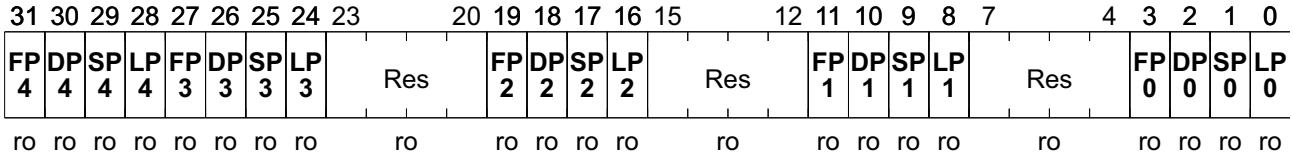
ChipID	Offset	Reset Value
Chip Identifier Register	00_H	$0007\ 1022_H$



Field	Bits	Type	Description
ID	31:4	ro	**Chip Identifier Register** $000\ 7102_H$ **ID** Chip Identifier
Ver	3:0	ro	**Version No** 2_H **Ver** Version No.

Port Status Register 0

PortStat_0 | **Offset** | **Reset Value**
Port Status Register 0 | **01_H** | **$0000\ 0000_H$**

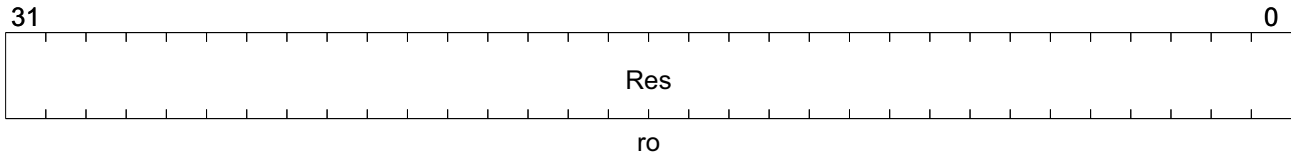


Field	Bits	Type	Description
FP4	31	ro	**Port 4 Flow Control Enable** 0_B **D** Flow Control Disable 1_B **FC4** 802.3X on for full duplex or back pressure on for half duplex.
DP4	30	ro	**Port 4 Duplex Status** 0_B **H** Half Duplex 1_B **F** Full Duplex
SP4	29	ro	**Port 4 Speed Status** 0_B **10** 10 Mbit/s 1_B **100** 100 Mbit/s
LP4	28	ro	**Port 4 Linkup Status** 0_B **NE** Link is not established. 1_B **E** Link is established.
FP3	27	ro	**Port 3 Flow Control Enable** 0_B **D** Flow Control Disable 1_B **FC3** 802.3X on for full duplex or back pressure on for half duplex.
DP3	26	ro	**Port 3 Duplex Status** 0_B **H** Half Duplex 1_B **F** Full Duplex
SP3	25	ro	**Port 3 Speed Status** 0_B **10** 10 Mbit/s 1_B **100** 100 Mbit/s
LP3	24	ro	**Port 3 Linkup Status** Port 3 Linkup Status: 0_B **N** Link is not established. 1_B **E** Link is established.
Res	23:20	ro	**Reserved**
FP2	19	ro	**Port 2 Flow Control Enable** 0_B **D** Flow Control Disable 1_B **FC2** 802.3X on for full duplex or back pressure on for half duplex.
DP2	18	ro	**Port 2 Duplex Status** 0_B **H** Half Duplex 1_B **F** Full Duplex
SP2	17	ro	**Port 2 Speed Status** 0_B **10** 10 Mbit/s 1_B **100** 100 Mbit/s

Field	Bits	Type	Description
LP2	16	ro	**Port 2 Linkup Status** Port 2 Linkup Status: 0_B **NE** Link is not established. 1_B **E** Link is established.
Res	15:12	ro	**Reserved**
FP1	11	ro	**Port 1 Flow Control Enable** 0_B **D** Flow Control Disable 1_B **FC1** 802.3X on for full duplex or back pressure on for half duplex.
DP1	10	ro	**Port 1 Duplex Status** 0_B **H** Half Duplex 1_B **F** Full Duplex
SP1	9	ro	**Port 1 Speed Status** 0_B **10** 10 Mbit/s 1_B **100** 100 Mbit/s
LP1	8	ro	**Port 1 Linkup Status** 0_B **NE** Not established. 1_B **E** Established.
Res	7:4	ro	**Reserved**
FP0	3	ro	**Port 0 Flow Control Enable** 0_B **D** Flow Control Disable 1_B **FC0** 802.3X on for full duplex or back pressure on for half duplex.
DP0	2	ro	**Port 0 Duplex Status** 0_B **H** Half Duplex 1_B **F** Full Duplex
SP0	1	ro	**Port 0 Speed Status** 0_B **10** 10 Mbit/s 1_B **100** 100 Mbit/s
LP0	0	ro	**Port 0 Linkup Status** 0_B **NE** Not established. 1_B **E** Established.

Port Status Register 1

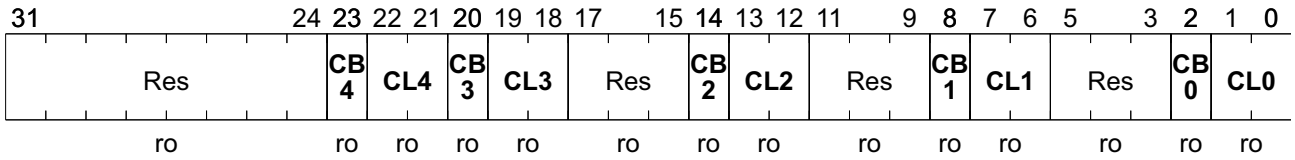
PortStat_1	Offset	Reset Value
Port Status Register 1	**02_H**	**$0000\ 0000_H$**



Field	Bits	Type	Description
Res	31:0	ro	**Reserved**

Cable Broken Status Register

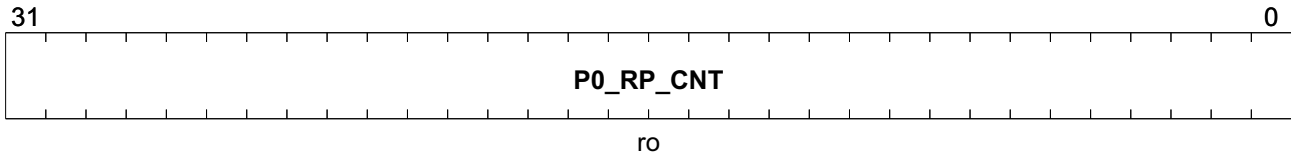
CabStat	Offset	Reset Value
Cable Broken Status	03_H	$0000\ 0000_H$



Field	Bits	Type	Description
Res	31:24	ro	**Reserved**
CB4	23	ro	**Port 4 Cable Broken**
CL4	22:21	ro	**Port 4 Cable Broken Length**
CB3	20	ro	**Port 3 Cable Broken**
CL3	19:18	ro	**Port 3 Cable Broken Length**
Res	17:15	ro	**Reserved**
CB2	14	ro	**Port 2 Cable Broken**
CL2	13:12	ro	**Port 2 Cable Broken Length**
Res	11:9	ro	**Reserved**
CB1	8	ro	**Port 1 Cable Broken**
CL1	7:6	ro	**Port 1 Cable Broken Length**
Res	5:3	ro	**Reserved**
CB0	2	ro	**Port 0 Cable Broken**
CL0	1:0	ro	**Port 0 Cable Broken Length**

Port 0 Receive Packet Count

P0_RP_CNT	Offset	Reset Value
Port 0 Receive Packet Count	04_H	$0000\ 0000_H$



Field	Bits	Type	Description
P0_RP_CNT	31:0	ro	**Counter**

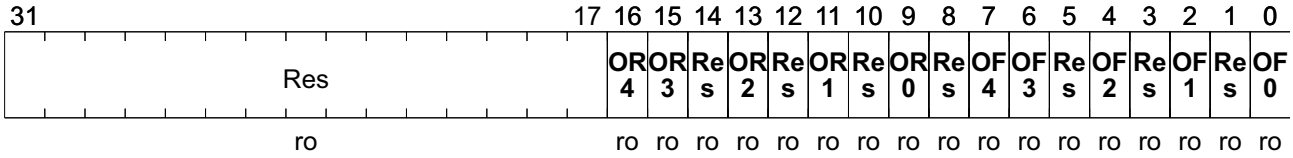
Similar Registers

Table 22 Per Port Counters

Register Short Name	Register Long Name	Offset Address	Page Number
P1_RP_CNT	Port 1 Receive Packet Count	06_H	
P2_RP_CNT	Port 2 Receive Packet Count	08_H	
P3_RP_CNT	Port 3 Receive Packet Count	$0A_H$	
P4_RP_CNT	Port 4 Receive Packet Count	$0B_H$	
P5_RP_CNT	Port 5 Receive Packet Count	$0C_H$	
P0_RB_CNT	Port 0 Receive Byte Count	$0D_H$	
P1_RB_CNT	Port 1 Receive Byte Count	$0F_H$	
P2_RB_CNT	Port 2 Receive Byte Count	11_H	
P3_RB_CNT	Port 3 Receive Byte Count	13_H	
P4_RB_CNT	Port 4 Receive Byte Count	14_H	
P5_RB_CNT	Port 5 Receive Byte Count	15_H	
P0_TP_CNT	Port 0 Transmit Packet Count	16_H	
P1_TP_CNT	Port 1 Transmit Packet Count	18_H	
P2_TP_CNT	Port 2 Transmit Packet Count	$1A_H$	
P3_TP_CNT	Port 3 Transmit Packet Count	$1C_H$	
P4_TP_CNT	Port 4 Transmit Packet Count	$1D_H$	
P5_TP_CNT	Port 5 Transmit Packet Count	$1E_H$	
P0_TB_CNT	Port 0 Transmit Byte Count	$1F_H$	
P1_TB_CNT	Port 1 Transmit Byte Count	21_H	
P2_TB_CNT	Port 2 Transmit Byte Count	23_H	
P3_TB_CNT	Port 3 Transmit Byte Count	25_H	
P4_TB_CNT	Port 4 Transmit Byte Count	26_H	
P5_TB_CNT	Port 5 Transmit Byte Count	27_H	
P0_COL_CNT	Port 0 Collision Count	28_H	
P1_COL_CNT	Port 1 Collision Count	$2A_H$	
P2_COL_CNT	Port 2 Collision Count	$2C_H$	
P3_COL_CNT	Port 3 Collision Count	$2E_H$	
P4_COL_CNT	Port 4 Collision Count	$2F_H$	
P5_COL_CNT	Port 5 Collision Count	30_H	
P0_ERR_CNT	Port 0 Error Count	31_H	
P1_ERR_CNT	Port 1 Error Count	33_H	
P2_ERR_CNT	Port 2 Error Count	35_H	
P3_ERR_CNT	Port 3 Error Count	37_H	
P4_ERR_CNT	Port 4 Error Count	38_H	
P5_ERR_CNT	Port 5 Error Count	39_H	

Over Flow Flag Register 0

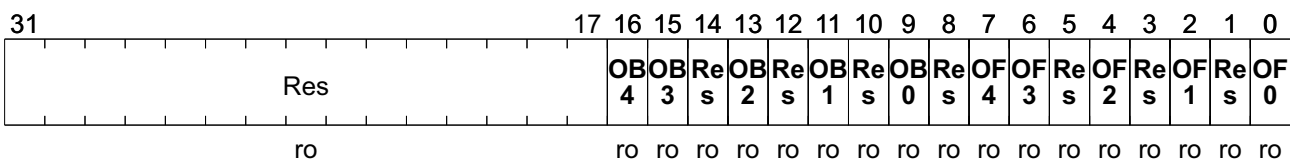
OverFlow_0 | **Offset** | **Reset Value**
Over Flow Flag Register 0 | **$3A_H$** | **$0000\ 0000_H$**



Field	Bits	Type	Description
Res	31:17	ro	**Reserved**
OR4	16	ro	**Overflow of Port 4 Receive Packet Byte Count**
OR3	15	ro	**Overflow of Port 3 Receive Packet Byte Count**
Res	14	ro	**Reserved**
OR2	13	ro	**Overflow of Port 2 Receive Packet Byte Count**
Res	12	ro	**Reserved**
OR1	11	ro	**Overflow of Port 1 Receive Packet Byte Count**
Res	10	ro	**Reserved**
OR0	9	ro	**Overflow of Port 0 Receive Packet Byte Count**
Res	8	ro	**Reserved**
OF4	7	ro	**Overflow of Port 4 Receive Packet Count**
OF3	6	ro	**Overflow of Port 3 Receive Packet Count**
Res	5	ro	**Reserved**
OF2	4	ro	**Overflow of Port 2 Receive Packet Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Receive Packet Count**
Res	1	ro	**Reserved**
OF0	0	ro	**Overflow of Port 0 Receive Packet Count**

Over Flow Flag Register 1

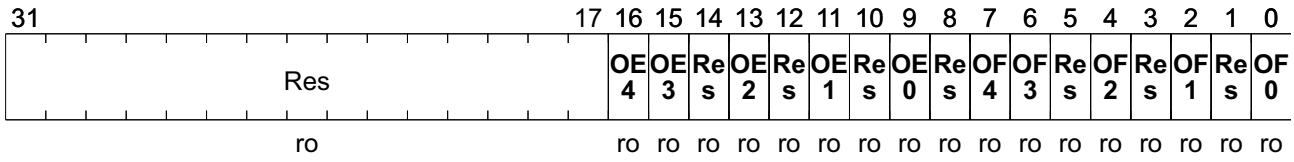
OverFlow_1 | **Offset** | **Reset Value**
Over Flow Flag Register 1 | **$3B_H$** | **$0000\ 0000_H$**



Field	Bits	Type	Description
Res	31:17	ro	**Reserved**
OB4	16	ro	**Overflow of Port 4 Transmit Packet Byte Count**
OB3	15	ro	**Overflow of Port 3 Transmit Packet Byte Count**
Res	14	ro	**Reserved**
OB2	13	ro	**Overflow of Port 2 Transmit Packet Byte Count**
Res	12	ro	**Reserved**
OB1	11	ro	**Overflow of Port 1 Transmit Packet Byte Count**
Res	10	ro	**Reserved**
OB0	9	ro	**Overflow of Port 0 Transmit Packet Byte Count**
Res	8	ro	**Reserved**
OF4	7	ro	**Overflow of Port 4 Transmit Packet Count**
OF3	6	ro	**Overflow of Port 3 Transmit Packet Count**
Res	5	ro	**Reserved**
OF2	4	ro	**Overflow of Port 2 Transmit Packet Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Transmit Packet Count**
Res	1	ro	**Reserved**
OF0	0	ro	**Overflow of Port 0 Transmit Packet Count**

Over Flow Flag Register 2

OverFlow_2	Offset	Reset Value
Over Flow Flag Register 2	**$3C_H$**	**$0000\ 0000_H$**



Field	Bits	Type	Description
Res	31:17	ro	**Reserved**
OE4	16	ro	**Overflow of Port 4 Error Count**
OE3	15	ro	**Overflow of Port 3 Error Count**
Res	14	ro	**Reserved**
OE2	13	ro	**Overflow of Port 2 Error Count**
Res	12	ro	**Reserved**
OE1	11	ro	**Overflow of Port 1 Error Count**
Res	10	ro	**Reserved**
OE0	9	ro	**Overflow of Port 0 Error Count**

Field	Bits	Type	Description
Res	8	ro	**Reserved**
OF4	7	ro	**Overflow of Port 4Collision Count**
OF3	6	ro	**Overflow of Port 3Collision Count**
Res	5	ro	**Reserved**
OF2	4	ro	**Overflow of Port 2 Collision Count**
Res	3	ro	**Reserved**
OF1	2	ro	**Overflow of Port 1 Collision Count**
Res	1	ro	**Reserved**
OF0	0	ro	**Overflow of Port 0 Collision Count**

4.3 Packet with Priority: Normal Packet Content

Table 23 Ethernet Packet from Layer 2

Preamble/SFD	Destination (6 bytes)	Source (6 bytes)	Packet length (2 bytes)	Data (46-1500 bytes)	CRC (4 bytes)
	Byte 0~5	Byte 6~11	Byte 12~13	Byte 14~	

4.4 VLAN Packet

Table 24 VLAN Packet

Tag Protocol TD 8100	Tag Control Information TCI	LEN Length	Routing Information
Byte 12~13	Byte14~15	Byte 16~17	Byte 18

Note: Samurai-5LC/5LCX (ADM6995LC/LCX) will check packet byte 12 &13. If byte[12:13]=8100h then this packet is a VLAN packet

Byte 14~15: Tag Control Information TCI

Bit[15:13]: User Priority 7~0

Bit 12: Canonical Format Indicator (CFI)

Bit[11~0]: VLAN ID. The Samurai-5LC/5LCX (ADM6995LC/LCX) will use bit[3:0] as VLAN group.

4.5 TOS IP Packet

Table 25 IP Packet

Type 0800	IP Header
Byte 12~13	Byte 14~15

Note: Samurai-5LC/5LCX (ADM6995LC/LCX) checks bytes 12 &13. If this value is 0800h then the Samurai-5LC/5LCX (ADM6995LC/LCX) knows this is a TOP priority packet.

IP header define

Byte 14

Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type

Bit[7~5]: IP Priority (Precedence) from 7~0

Bit 4: No Delay (D)

Bit 3: High Throughput

Bit 2: High Reliability (R)

Bit[1:0]: Reserved

4.6 EEPROM Access

Customer can select Samurai-5LC/5LCX (ADM6995LC/LCX) read EEPROM contents as chip setting or not. Samurai-5LC/5LCX (ADM6995LC/LCX) will check the signature of EEPROM to decide read content of EEPROM or not.

Table 26 RESETL & EEPROM content relationship

RESETL	CS	SK	DI	DO
0	High Impedance	High Impedance	High Impedance	High Impedance
Rising edge 01 (30ms)	Output	Output	Output	Input
1 (after 30ms)	Input	Input	Output	Input

Keep at least 30ms after RESETL from 01. Samurai-5LC/5LCX (ADM6995LC/LCX) will read data from EEPROM. After RESETL if CPU updates EEPROM then Samurai-5LC/5LCX (ADM6995LC/LCX) will update configuration registers too.

When CPU programming EEPROM & Samurai-5LC/5LCX (ADM6995LC/LCX), Samurai-5LC/5LCX (ADM6995LC/LCX) recognizes the EEPROM WRITE instruction only. If there is any Protection instruction before or after the EEPROM WRITE instruction, CPU needs to generate separated CS signal cycles for each Protection & WRITE instruction.

CPU can directly program Samurai-5LC/5LCX (ADM6995LC/LCX) after 30ms of Reset signal rising edge with or without EEPROM

Samurai-5LC/5LCX (ADM6995LC/LCX) serial chips will latch hardware-reset value as recommend value. It includes EEPROM interface:

EECS: Internal Pull down 40K resister.

EESK: TP port Auto-MDIX select. Internal pull down 40K resister as non Auto-MDIX mode.

EDI: Dual Color Select. Internal pull down 40K resister as Single Color Mode.

EDO: EEPROM enable. Internal pull up 40K resister as EEPROM enable.

The below Figure is Samurai-5LC/5LCX (ADM6995LC/LCX) serial chips EEPROM pins operation at different stages. Reset signal is controlled by CPU with at least 100ms low. Point1 is Reset rising edge. CPU must prepare proper values on EECS(0), EESK, EDI, EDO(1) before this rising edge. Samurai-5LC/5LCX (ADM6995LC/LCX) will read this value into chip at Point2. CPU must keep these values over point2. Point2 is 200ns after Reset rising edge.

Samurai-5LC/5LCX (ADM6995LC/LCX) serial chips will read EEPROM content at Point4 which 800ns far away from the rising edge of Reset. CPU must turn EEPROM pins EECS, EESK, EDI and EDO to High-Z or pull high before Point4.

If users want to change the state to High-Z or pull high on EEPROM pins, the order is CS-> DI -> DO -> SK is better.

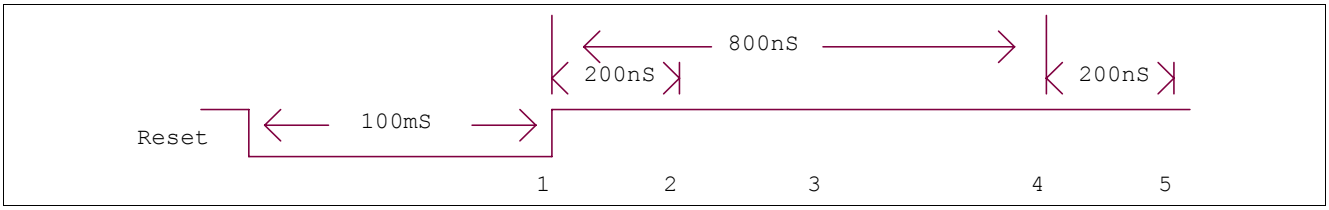


Figure 5 CPU Generated Reset Signal Requirement

A little bit different than the timing on writing EEPROM. See below graph. Must be careful when CS goes down after write a command, SK must issue at least one clock. This is the difference between Samurai-5LC/5LCX (ADM6995LC/LCX) with EEPROM write timing. If system is without EEPROM then users must write Samurai-5LC/5LCX (ADM6995LC/LCX) internal register by 93C66 timing. If user uses EEPROM then the writing timing is dependent on the EEPROM type.

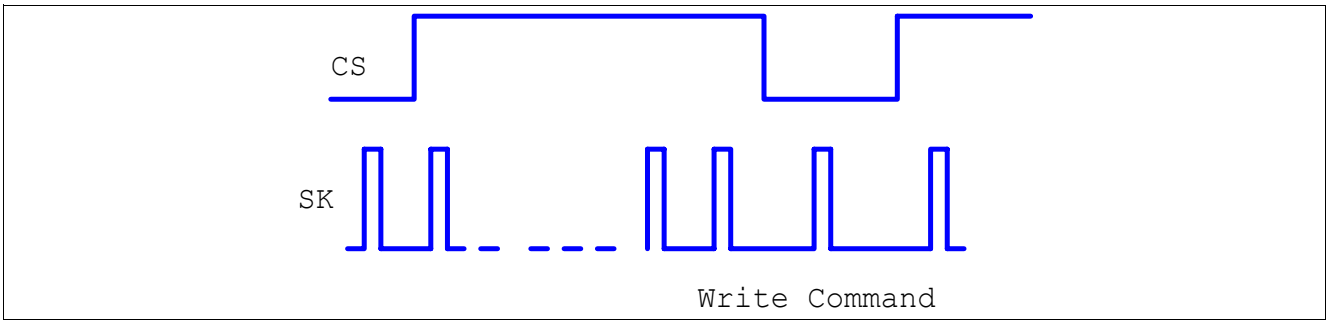


Figure 6 CPU Write EEPROM Command Requirement

4.7 Serial Interface Timing

Samurai-5LC/5LCX (ADM6995LC/LCX) serial chip's internal counter or EEPROM access timing

EESK: Similar to the MDC signal.

EDI: Similar to the MDIO signal

ECS: Must keep be kept low.

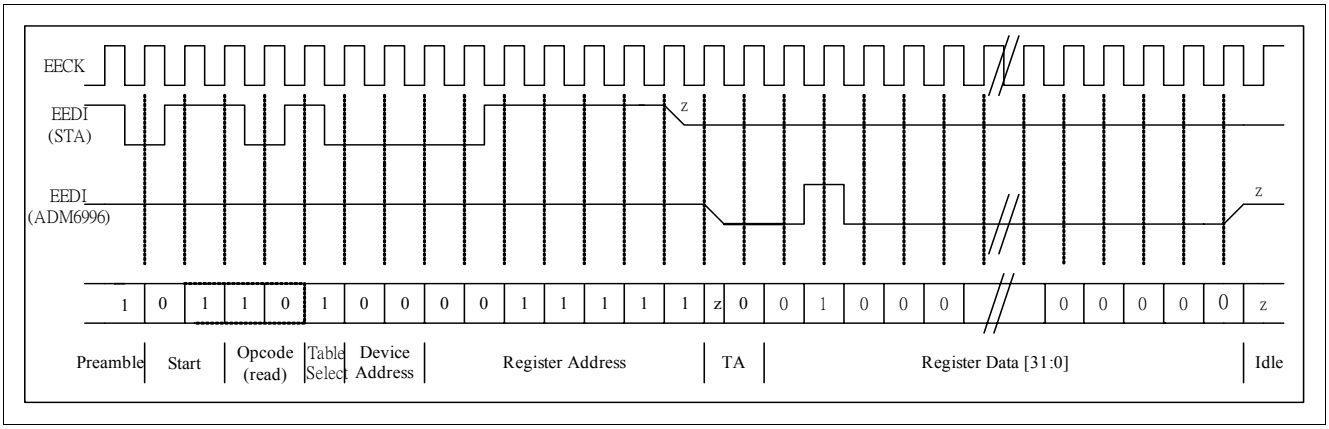


Figure 7 Serial Interface Read Command Timing

Preamble: At least 32 continuous 1_B's

Start: 01_B(2 bits)

Opcode: 10_B (2 bits, Only supports a read command)

Table select: 1_B = Counter, 0_B = EEPROM (1 bit)

Register Address: Read Target register address. (7 bits)

TA: Turn Around.

Register Data: 32 bit data.

Counter output bit sequence is bit 31 to bit 0.

If a user reads the EEPROM then 32 bits of data will separate as two EEPROM registers. The sequence is:

1. Register +1, Register (Register is even number)
2. Register, Register-1(Register is Odd number)

Example:

Read Register 00_H then the Samurai-5LC/5LCX (ADM6995LC/LCX) will drive 01_H & 00_H

Read Register 03_H then Samurai-5LC/5LCX (ADM6995LC/LCX) will drive 03_H & 02_H

Idle: EESK must send at least one clock pulse at idle time

Samurai-5LC/5LCX (ADM6995LC/LCX) issue Reset internal counter command

EESK: Similar to the MDC signal

EDI: Similar to the MDIO signal

ECS: Must keep low.

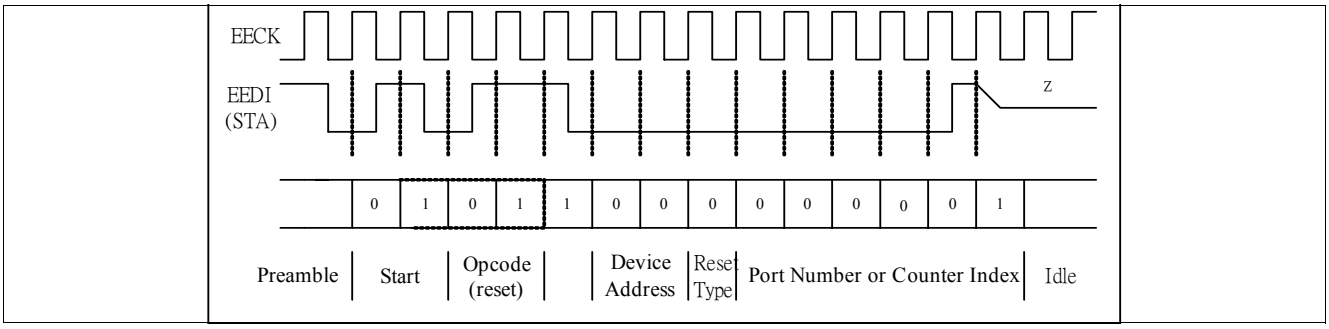


Figure 8 Serial Interface Reset Command Timing

Preamble: At least 32 continuous 1_B's

Start: 01_B(2 bits)

Opcode: 01_B (2 bits, Reset command)

Device Address: Chip physical address as PHYAS[1:0].

Reset_type: Reset the counter by port number or by counter index

1_B = Clear dedicate port's all counters

0_B = Clear dedicate counter

Port_number or counter index: User defines clear port or counter

Idle: EESK must send at least one clock pulse at idle time

5 Electrical Specification

5.1 TX/FX Interface

5.1.1 TP Interface

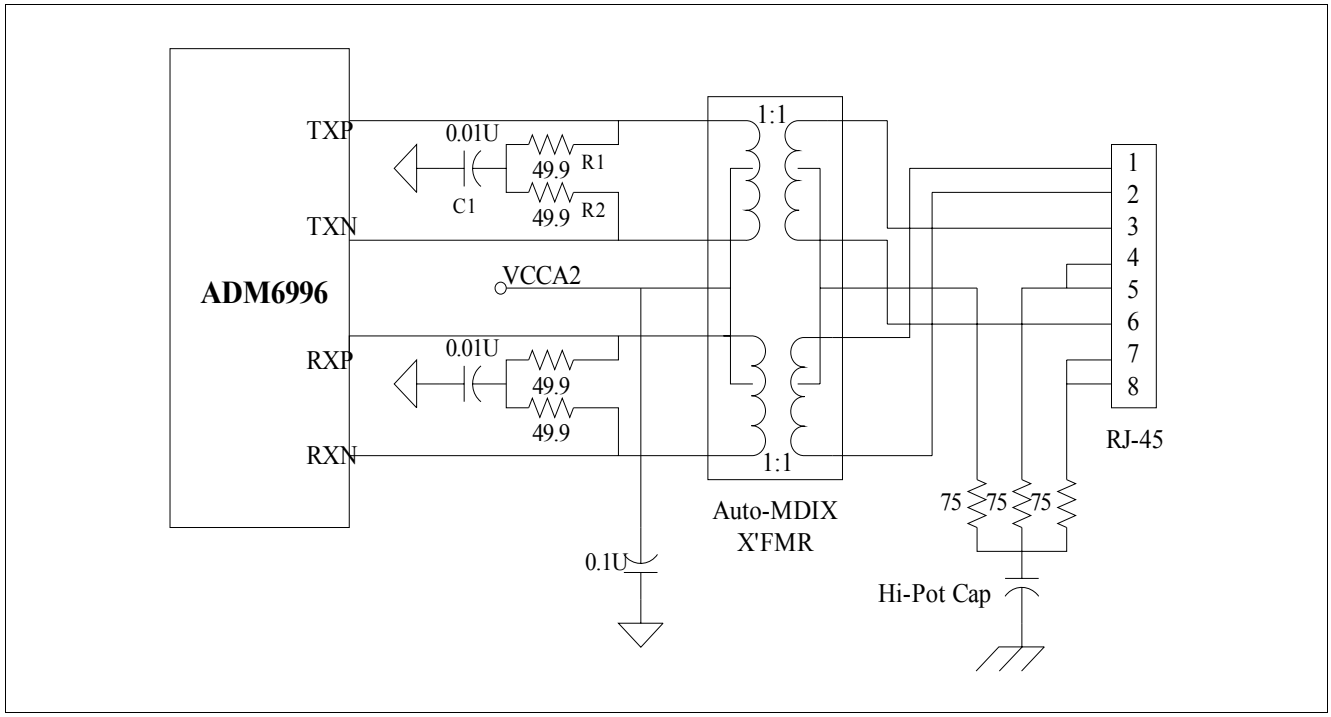


Figure 9 TP Interface

Transformer requirements:

- TX/RX rate 1:1
- TX/RX central tap connect together to VCCA2

Users can change the TX/RX pin for easy layout but do not change the polarity. Samurai-5LC/5LCX (ADM6995LC/LCX) supports auto polarity on the receiving side.

5.1.2 FX Interface

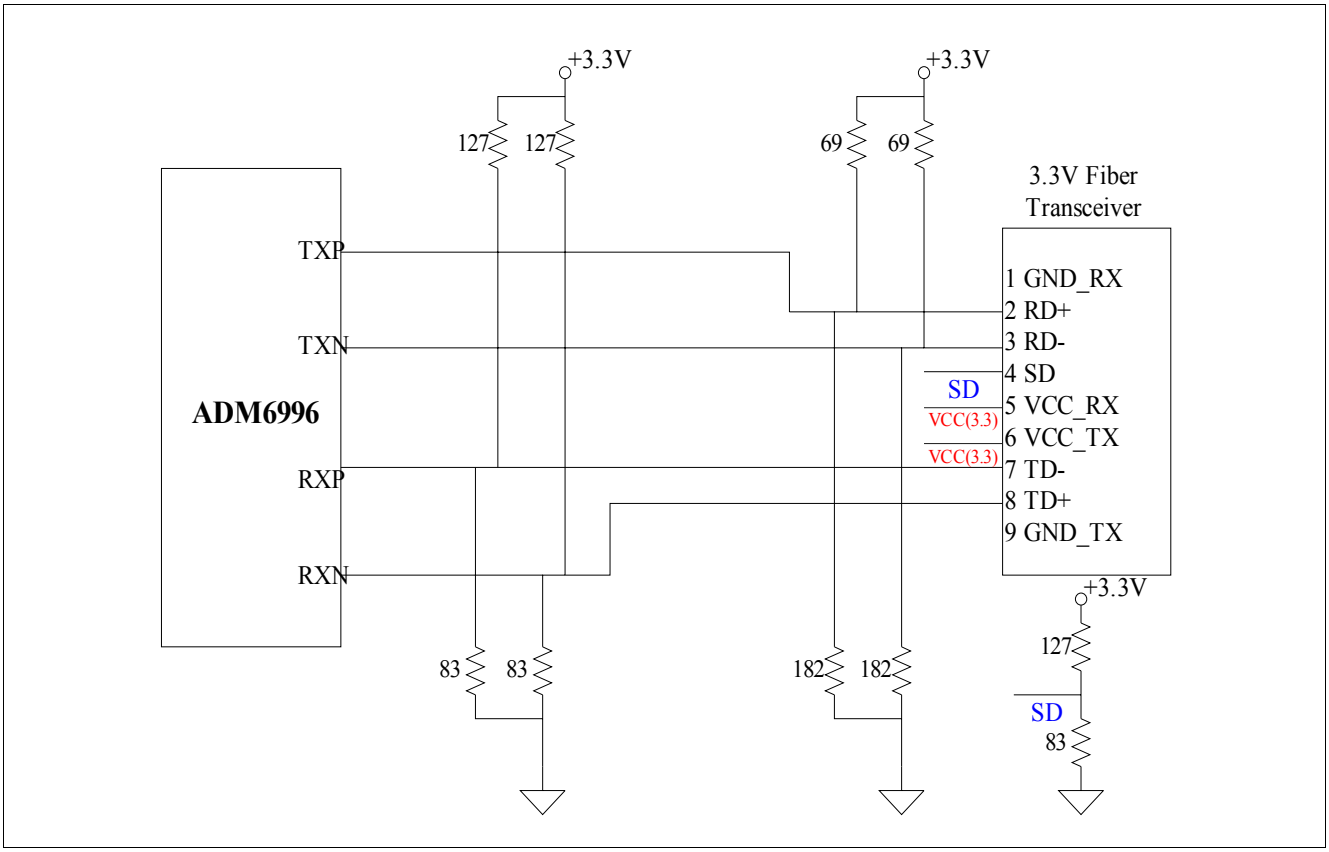


Figure 10 FX Interface

5.2 DC Characterization

Table 27 Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power consumption when all twisted pair ports are linked at 100 Mbit/s.	P_{100M_5TP}	–	980	–	mW	Under EEPROM Register 29_H = $C000_H$, and 30_H = 985_H
Power consumption when all twisted pair ports are linked at 10 Mbit/s (include transformer).	P_{10M_5TP}	–	1450	–	mW	Under EEPROM Register 29_H = $C000_H$, and 30_H = 985_H
Power consumption when all twisted pair ports are disconnected.	P_{DIS_5TP}	–	500	–	mW	Under EEPROM Register 29_H = $C000_H$, and 30_H = 985_H

Table 28 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Power Supply for I/O pad	V_{CC3O}	2.97	3.3	3.63	V	–
3.3 V Power Supply for bias circuit	V_{CCBS}	2.97	3.3	3.63	V	–
3.3 V Power Supply for A/D converter	V_{CCAD}	2.97	3.3	3.63	V	–
1.8 V Power Supply for line driver	V_{CCA2}	1.62	1.8	1.98	V	–
1.8 V Power Supply for PLL	V_{CCPLL}	1.62	1.8	1.98	V	–
1.8 V Power Supply for Digital core	V_{CCIK}	1.62	1.8	1.98	V	–
Input Voltage	V_{IN}	-0.3	–	V_{CC3O} + 0.3	V	–
Output Voltage	V_{out}	-0.3	–	V_{CC3O} + 0.3	V	–
Maximum current for 3.3 V power supply	$I_{3.3VMAX}$	–	–	100	mA	–
Maximum current for 1.8 V power supply (include transformer)	$I_{1.8VMAX}$	–	–	800	mA	–
Storage Temperature	T_{STG}	-55	–	155	°C	–
Thermal Resistance	$Theta_{JA}$		33.0		°C/W	ADM6995LC/LCX
	$Theta_{JC}$		14.9		°C/W	ADM6995LC/LCX
ESD Rating	ESD	1.0	–	–	kV	–

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 29 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Power Supply for I/O pad	V_{CC3O}	3.135	3.3	3.465	V	–
3.3 V Power Supply for bias circuit	V_{CCBS}	3.135	3.3	3.465	V	–
3.3 V Power Supply for A/D converter	V_{CCAD}	3.135	3.3	3.465	V	–
1.8 V Power Supply for line driver	V_{CCA2}	1.71	1.8	1.89	V	–
1.8 V Power Supply for PLL	V_{CCPLL}	1.71	1.8	1.89	V	–
1.8 V Power Supply for Digital core	V_{CCIK}	1.71	1.8	1.89	V	–

Table 29 Recommended Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Voltage	V_{in}	0	–	V_{CC}	V	–
Junction Operating Temperature	T_j	0	25	115	°C	–

Table 30 DC Electrical Characteristics for 3.3 V Operation[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	–	–	0.8	V	TTL
Input High Voltage	V_{IH}	2.0	–	–	V	TTL
Output Low Voltage	V_{OL}	–	–	0.4	V	TTL
Output High Voltage	V_{OH}	2.4	–	–	V	TTL
Input Pull-up/down Resistance	R_I	–	50	–	kΩ	V_{IL} = 0 V or V_{IH} = V_{cc3o}

1) Under V_{CC3O} = 2.97V ~ 3.63 V, T_j = 0 °C ~ 115 °C

5.3 AC Characterization

5.3.1 XTAL/OSC Timing

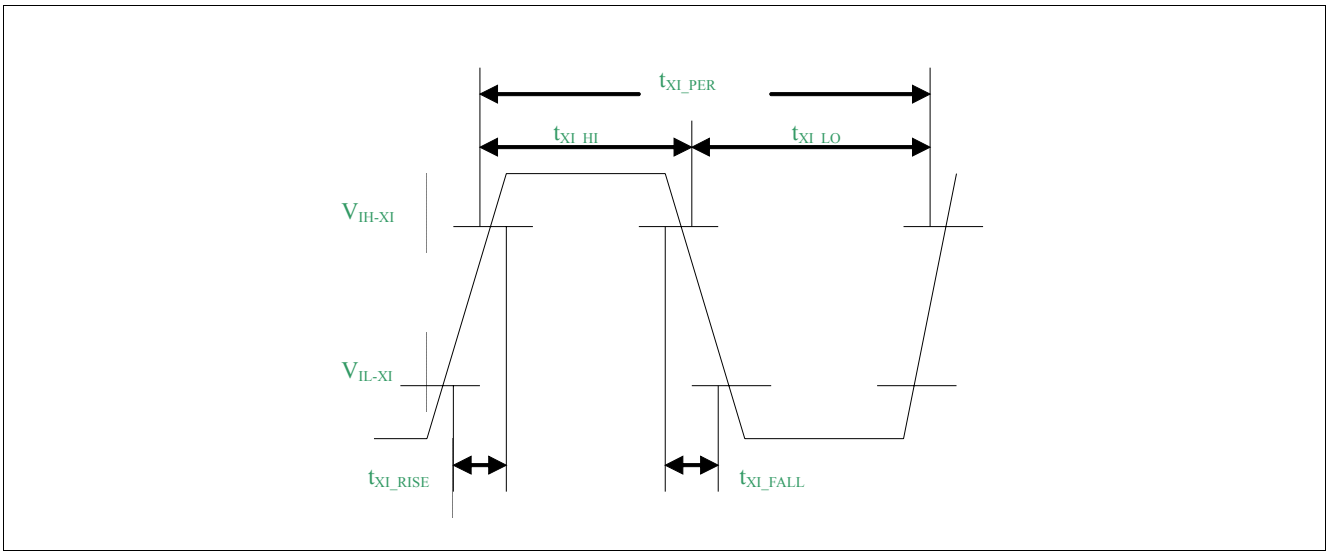


Figure 11 XTAL/OSC Timing

Table 31 XTAL/OSC Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
XI/OSCI Clock Period	$t_{\_XI\_PER}$	40.0 - 50ppm	40.0	40.0 + 50ppm	ns	–
XI/OSCI Clock High	$t_{\_XI\_HI}$	14	20.0	–	ns	–
XI/OSCI Clock Low	$t_{\_XI\_LO}$	14	20.0	–	ns	–
XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	$t_{\_XI\_RISE}$	–	–	4	ns	–
XI/OSCI Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	$t_{\_XI\_FALL}$	–	–	4	ns	–

5.3.2 Power On Reset

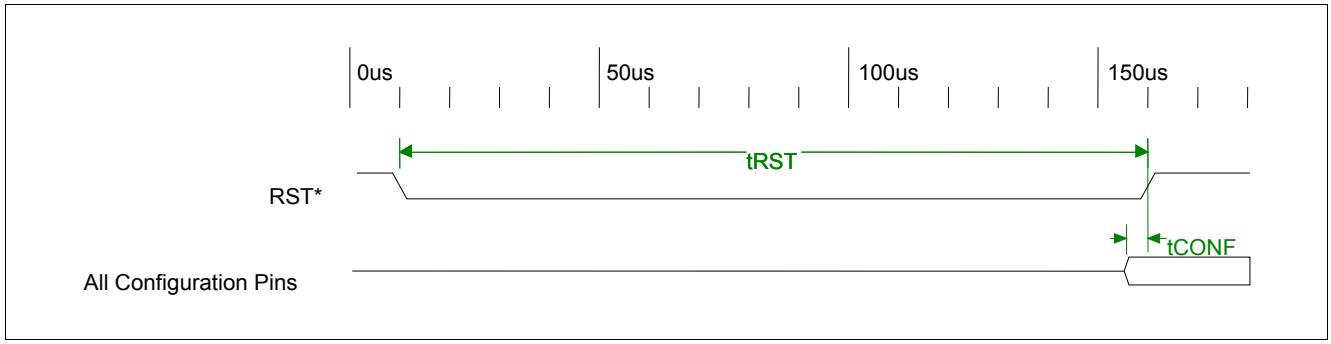


Figure 12 Power On Reset Timing

Table 32 Power On Reset Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RST Low Period	t_{RST}	100	–	–	ms	–
Start of Idle Pulse Width	t_{CONF}	100	–	–	ns	–

5.3.3 EEPROM Interface Timing

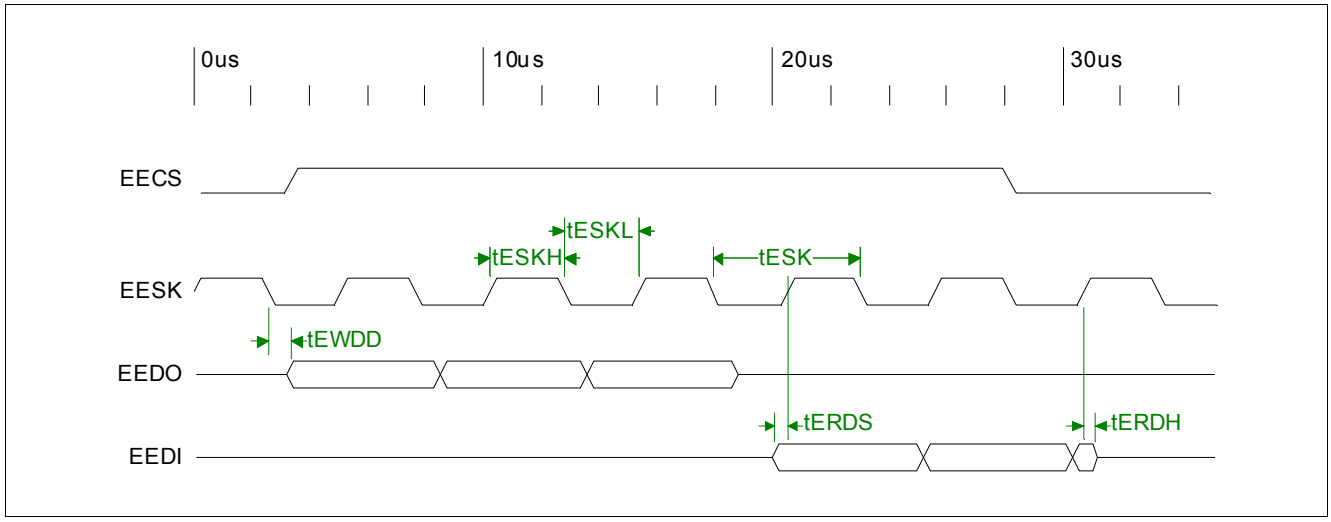


Figure 13 EEPROM Interface Timing

Table 33 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	t_{ESK}	–	5120	–	ns	–
EESK Low Period	t_{ESKL}	2550	–	2570	ns	–
EESK High Period	t_{ESKH}	2550	–	2570	ns	–
EEDI to EESK Rising Setup Time	t_{ERDS}	10	–	–	ns	–
EEDI to EESK Rising Hold Time	t_{ERDH}	10	–	–	ns	–
EESK Falling to EEDO Output Delay Time	t_{EWDD}	–	–	20	ns	–

5.3.4 SDC/SDIO Timing

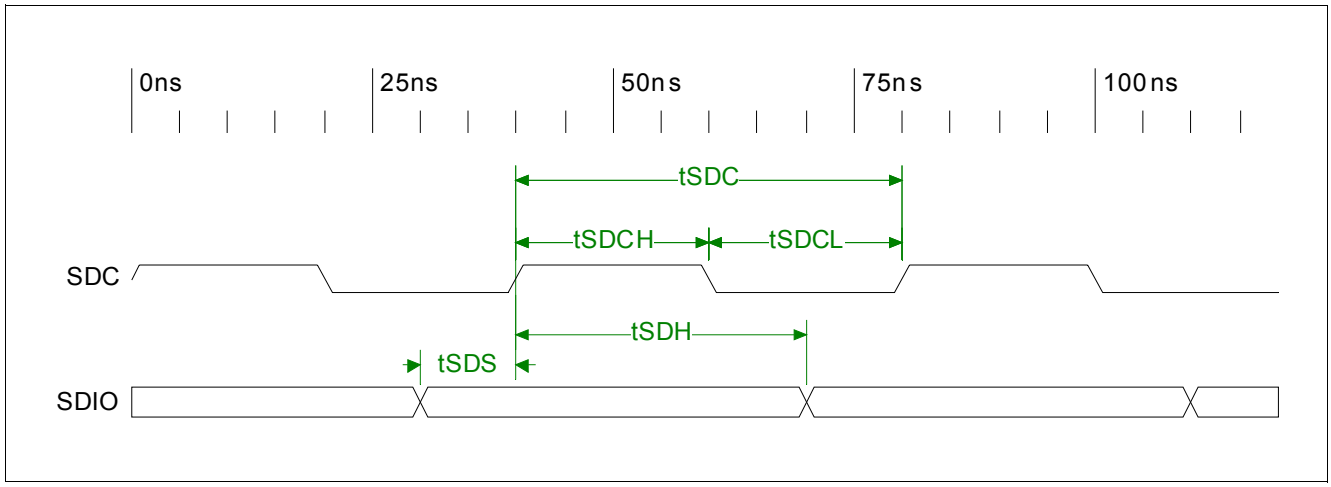
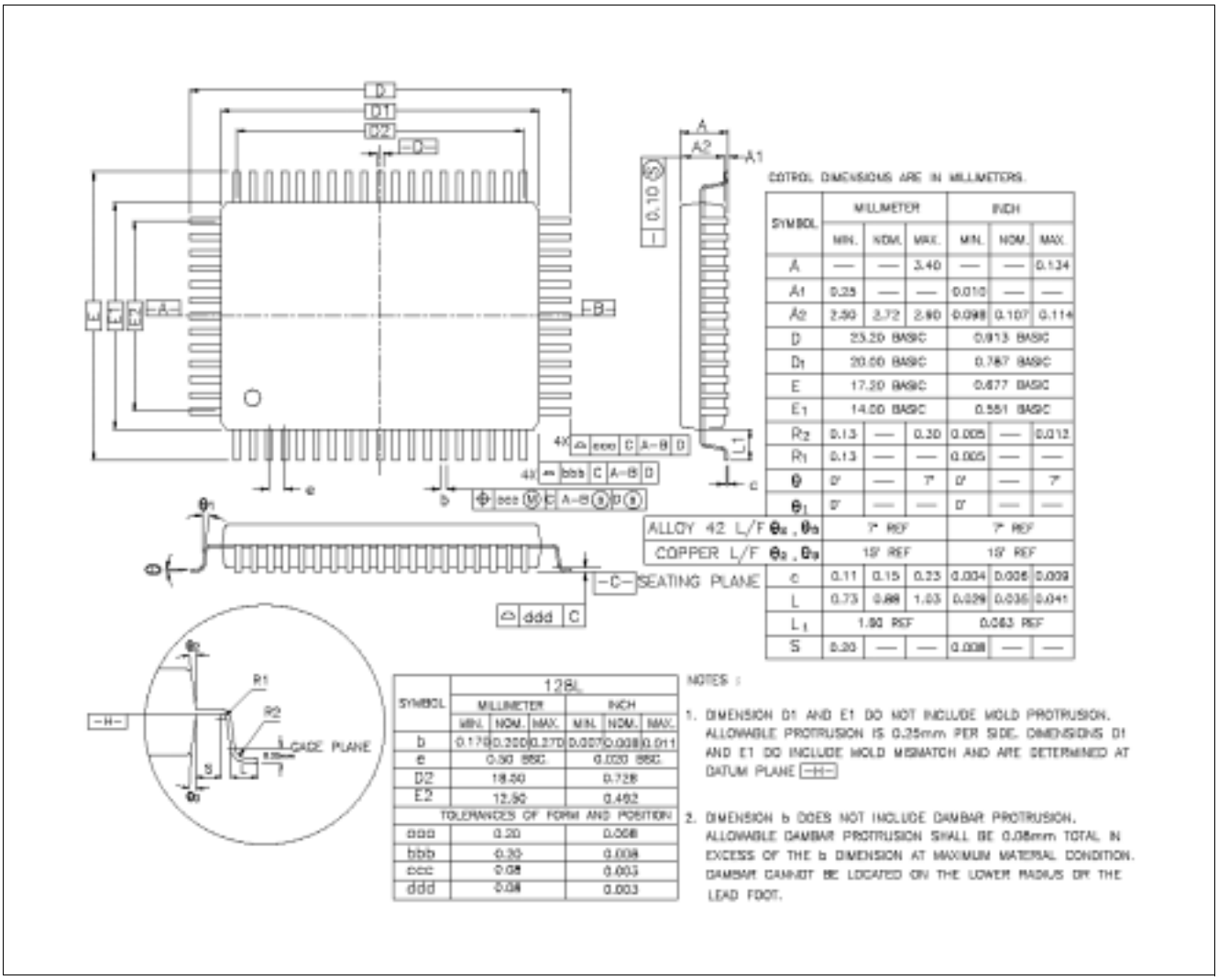


Figure 14 SDC/SDIO Timing

Table 34 SDC/SDIO Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDC Period	t_{CK}	20	–	–	ns	–
SDC Low Period	t_{CKL}	10	–	–	ns	–
SDC High Period	t_{CKH}	10	–	–	ns	–
SDIO to SDC rising setup time on read/write cycle	t_{SDS}	4	–	–	ns	–
SDIO to SDC rising hold time on read/write cycle	t_{SDH}	2	–	–	ns	–

6 Package Outlines



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.90	3.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
ALLOY 42 L/F θ2 , θ3	7° REF			7° REF		
COPPER L/F θ2 , θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.80 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	128L			
	MILLIMETER		INCH	
	MIN.	NOM. MAX.	MIN.	NOM. MAX.
b	0.17	0.22 0.27	0.007	0.009 0.011
e	0.50 BSC		0.020 BSC	
D2	18.50		0.728	
E2	12.50		0.492	
TOLERANCES OF FORM AND POSITION				
aaa	0.20		0.008	
bbb	0.30		0.012	
ccc	0.08		0.003	
ddd	0.08		0.003	

Figure 15 P-PQFP-128 Outside Dimension

6.1 Package Information

Product Name	Product Type	Package
5-Port 10/100 Mbit/s Single Chip Ethernet Switch Controller	Samurai-5LC/LCX, ADM6995LC/LCX-AD-T-1, Version AD	P-PQFP-128

Terminology

B	
BER	Bit Error Rate
C	
CFI	Canonical Format Indicator
COL	Collision
CRC	Cyclic Redundancy Check
CRS	Carrier Sense
CS	Chip Select
D	
DA	Destination Address
DI	Data Input
DO	Data Output
E	
EDI	EEPROM Data Input
EDO	EEPROM Data Output
EECS	EEPROM Chip Select
EESK	EEPROM Clock
ESD	End of Stream Delimiter
F	
FEFI	Far End Fault Indication
FET	Field Effect Transistor
FLP	Fast Link Pulse
G	
GND	Ground
GPSI	General Purpose Serial Interface
I	
IPG	Inter-Packet Gap
L	
LFSR	Linear Feedback Shift Register
M	
MAC	Media Access Controller
MDIX	MDI Crossover
MII	Media Independent Interface
N	
NRZI	Non Return to Zero Inverter
NRZ	Non Return to Zero
P	
PCS	Physical Coding Sub-layer
PHY	Physical Layer
PLL	Phase Lock Loop
PMA	Physical Medium Attachment

PMD	Physical Medium Dependent
Q	
QoS	Quality of Service
QFP	Quad Flat Package
R	
RST	Reset
RXCLK	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid
RXER	Receive Data Errors
RXN	Receive Negative (Analog receive differential signal)
RXP	Receive Positive (Analog receive differential signal)
S	
SA	Source Address
SOHO	Small Office Home Office
SSD	Start of Stream Delimiter
SQE	Signal Quality Error
T	
TOS	Type of Service
TP	Twisted Pair
TTL	Transistor Logic
TXCLK	Transmission Clock
TXD	Transmission Data
TXEN	Transmission Enable
TXN	Transmission Negative
TXP	Transmission Positive

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